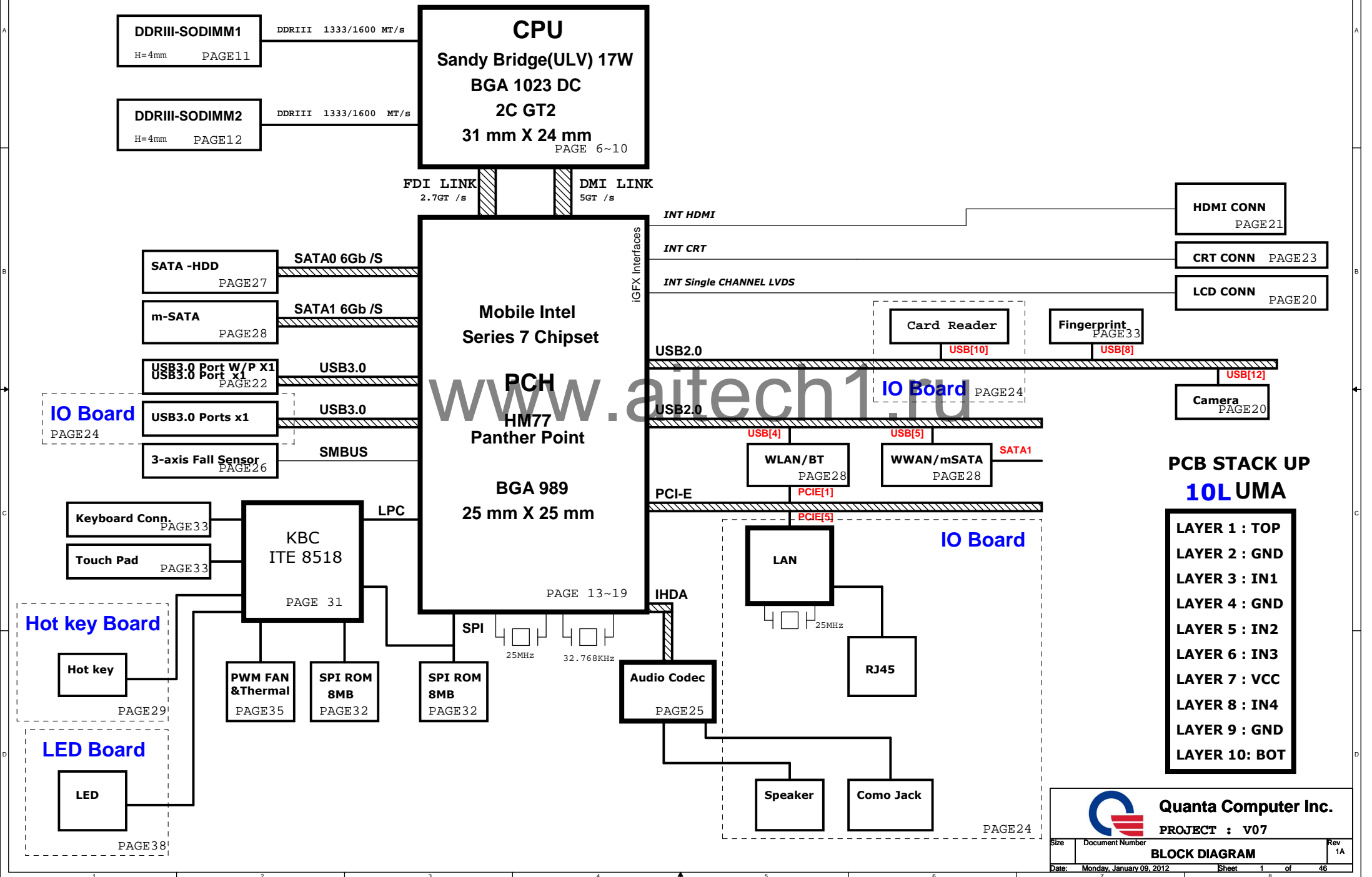


# V07 BLOCK DIAGRAM



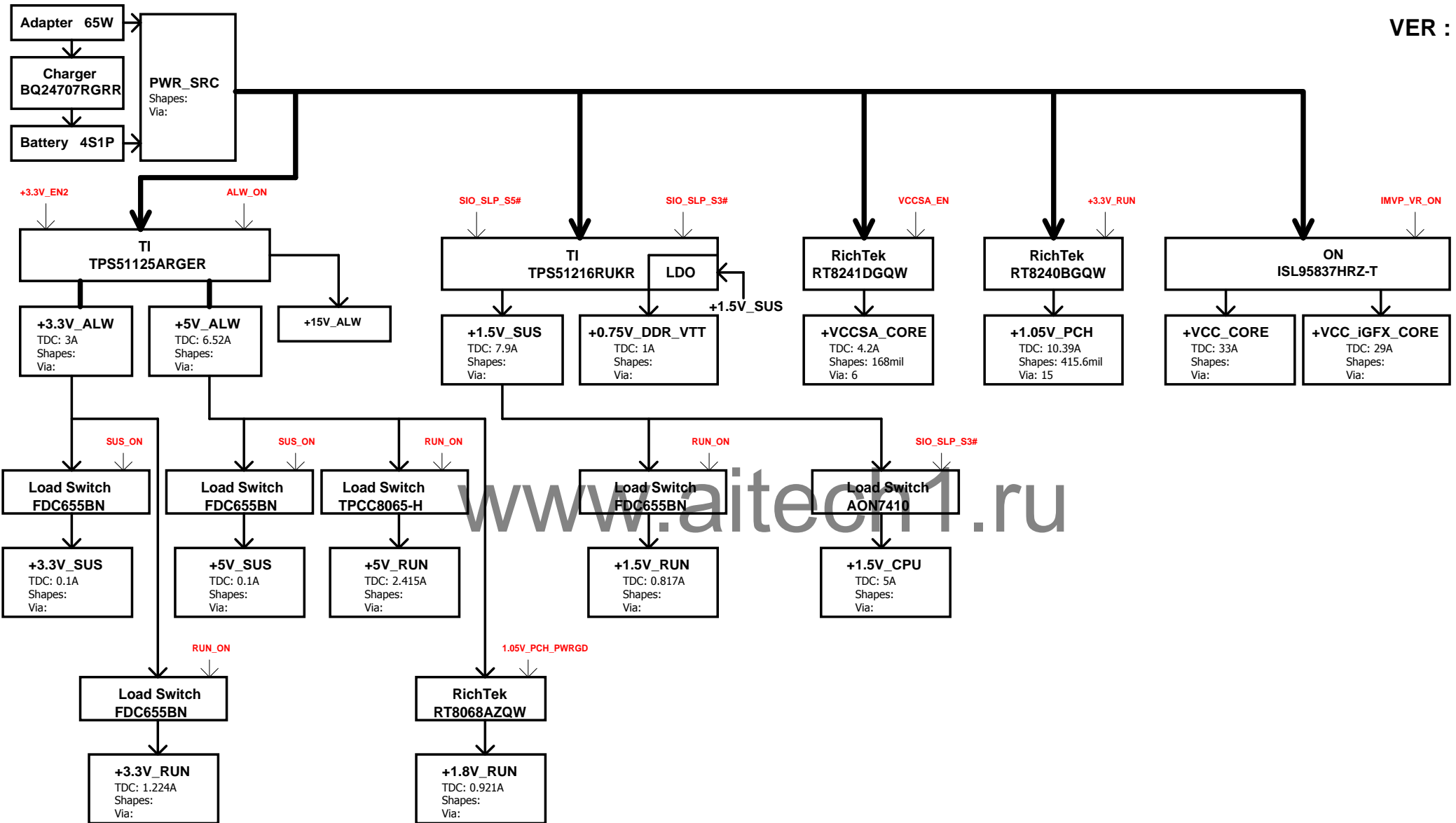


USB Master	Port Assignment
USB0	External port#1 (USB3.0)
USB1	External port#2 (USB3.0/eSATA/ Power share/ debug port)
USB2	External port#3 (USB3.0)
USB3	External port#4 (USB3.0) (NC)
USB4	MiniCard 1 (WLAN/BT/WiMAX)
USB5	MiniCard 2 (WWAN)
USB6	X(FOR HM77)
USB7	X(FOR HM77)
USB8	Fingerprint
USB9	Touch panel (NC, for debug)
USB10	Card Reader
USB11	Express Card (NC)
USB12	Camera
USB13	NC

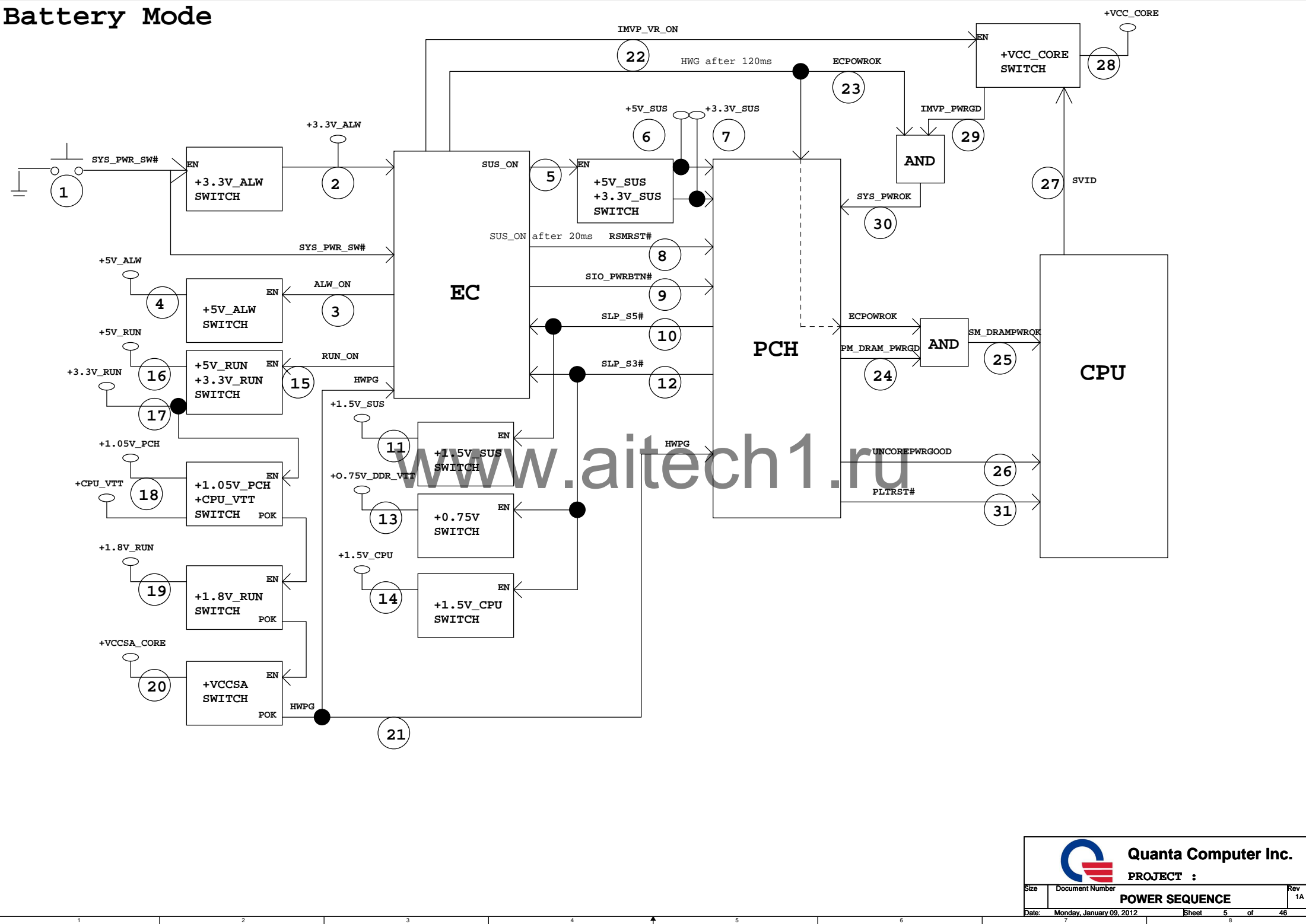
SATA Master	Port Assignment
SATA0	HDD
SATA1	mSATA
SATA2	NC
SATA3	ODD (NC)
SATA4	eSATA (NC)
SATA5	NC

PCIE Master	Port Assignment
PCIE 1	WLAN
PCIE 2	WWAN (NC)
PCIE 3	Card reader (NC)
PCIE 4	NC
PCIE 5	LAN
PCIE 6	Express card (NC)
PCIE 7	NC
PCIE 8	NC

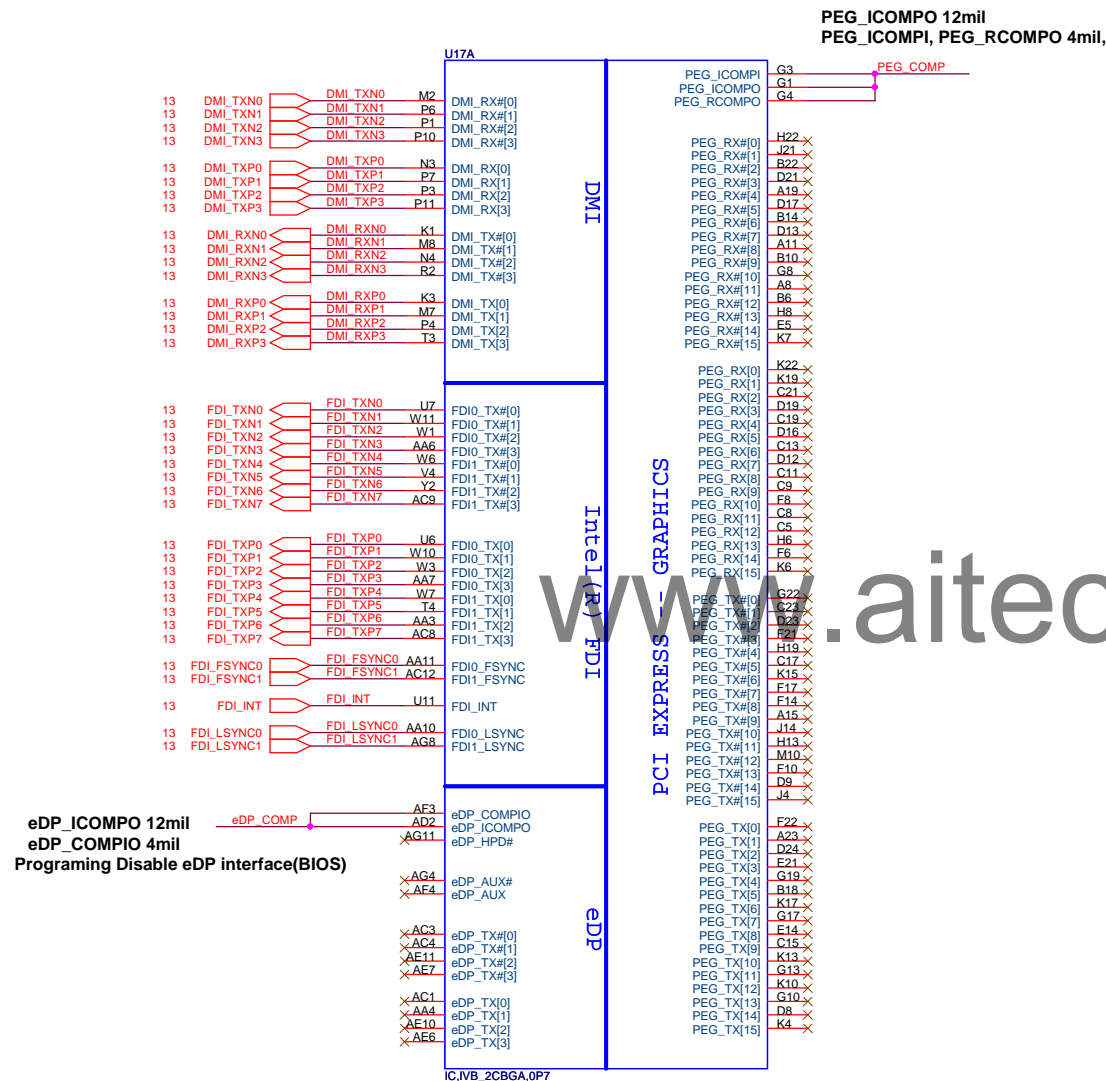
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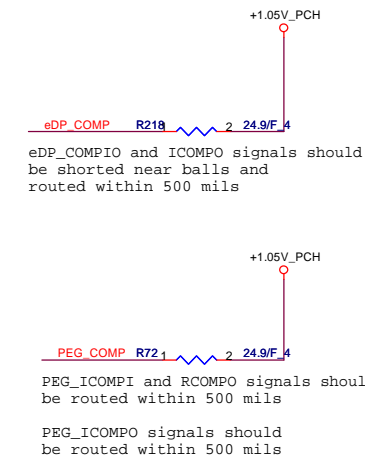
# Battery Mode



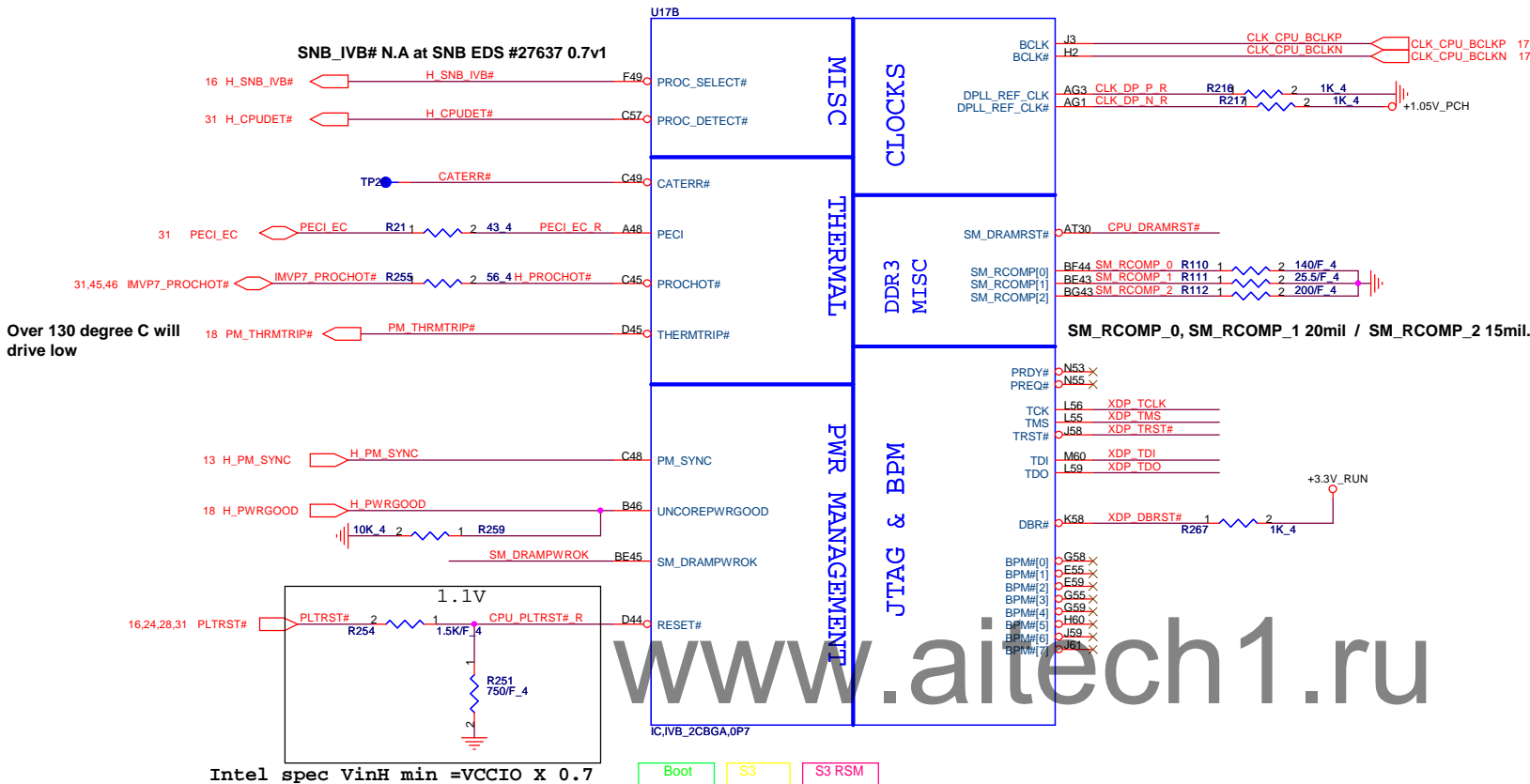
# Ivy Bridge Processor (RESERVED, CFG)



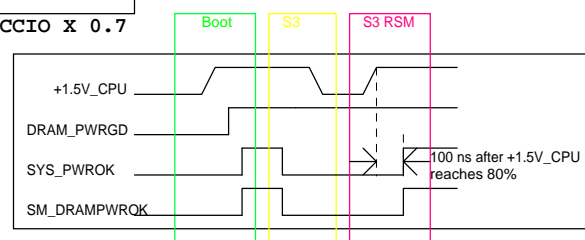
## DP & PEG Compensation



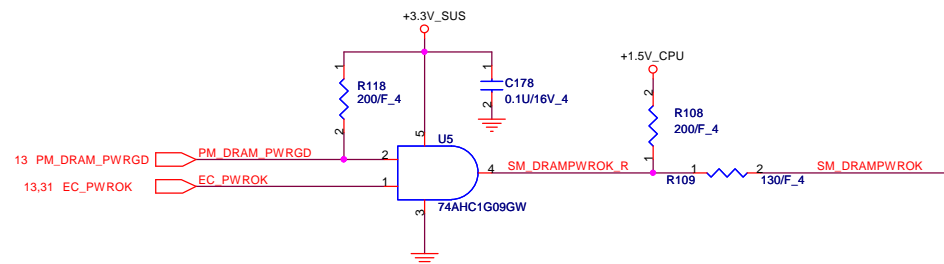
# Ivy Bridge Processor (CLK,MISC,JTAG)



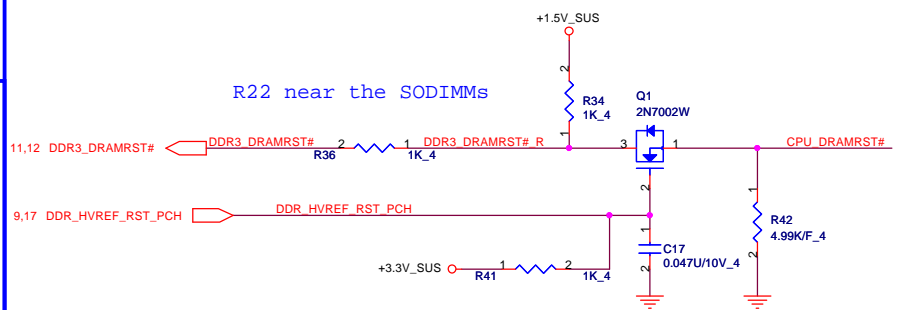
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Follow #DG1.0 436735 P105  
DDR Power Gating Topology

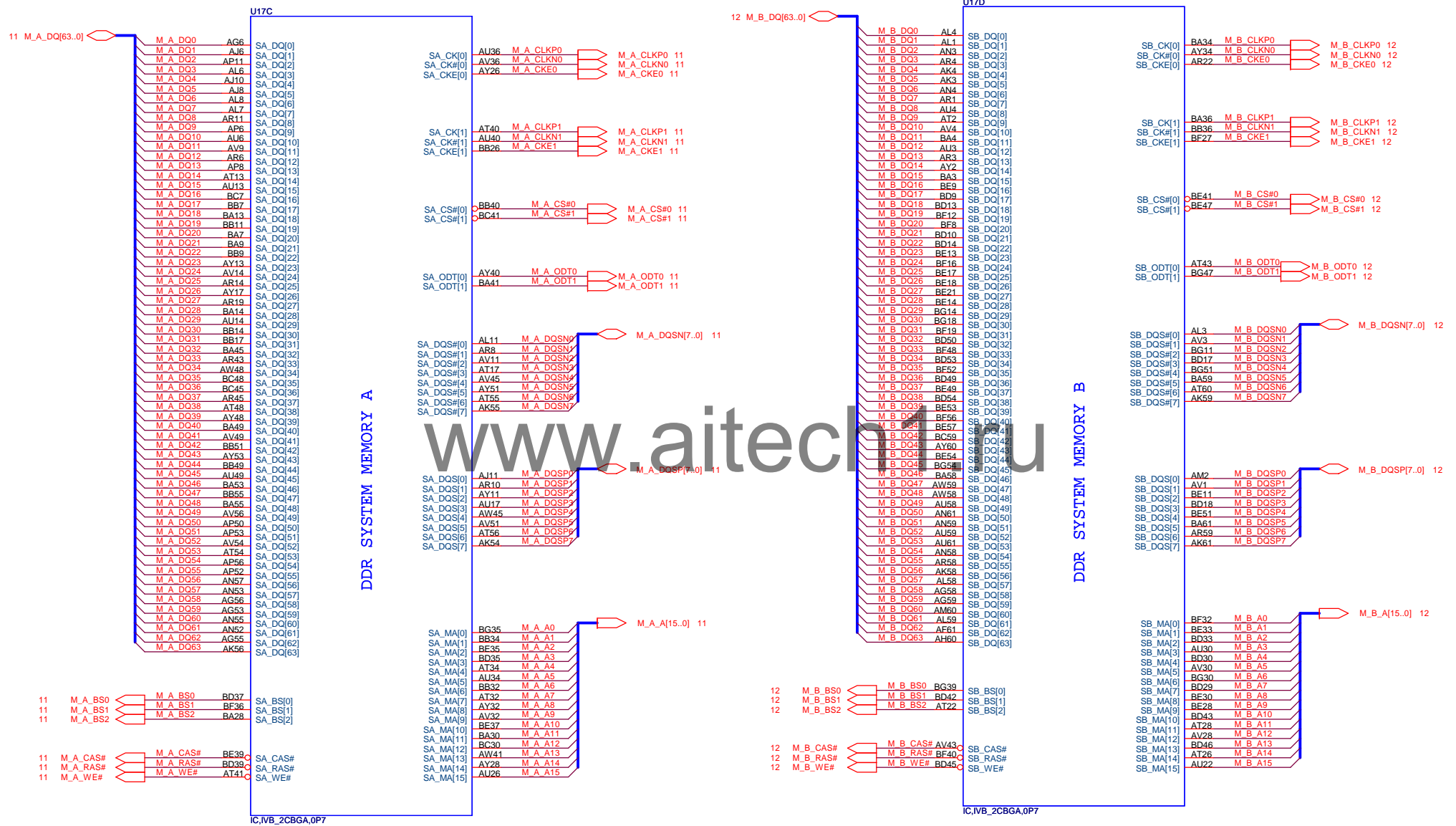


Follow #DG1.0 436735 P107  
DRAMRST# Routing Illustration



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**PROJECT : V07**

# Ivy Bridge Processor (DDR3)

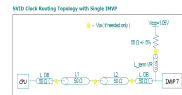


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PROJECT : V07



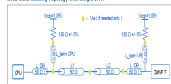
**CPU Core Power**  
**SNB: 33A**  
**IVY: 33A**  
**10uF x 11**  
**1uF x15**



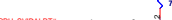
## SVID CLK



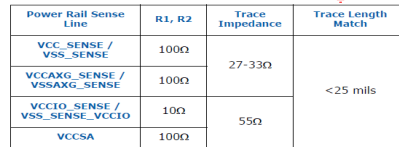
SVID D



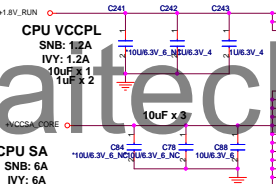
**SVID ALERT**



SNB: 8.5A  
IVY: 8.5A  
10uF x12

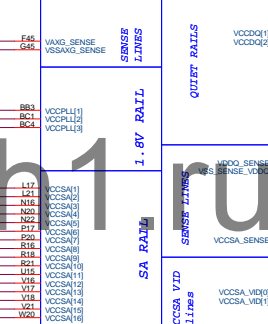


SNB: 29A  
IVY: 29A  
10uF x 12

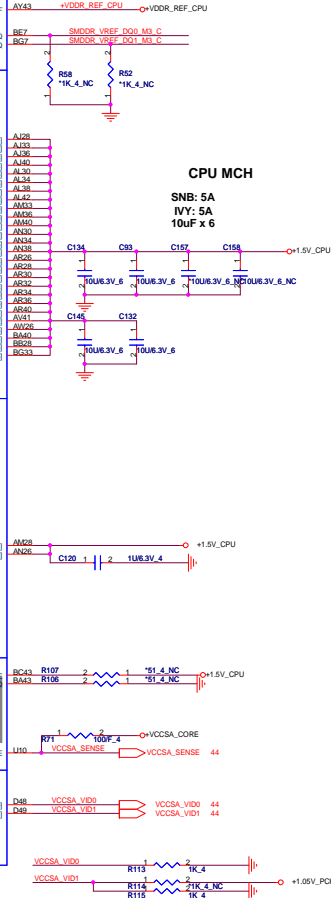


CPU SA  
SNB: 6A  
IVY: 6A

## POWER

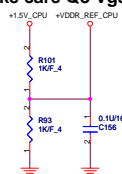


CAD Note: +VDDR\_REF\_CPU should have 10 mil trace width



Q11  
S3 Power reduce

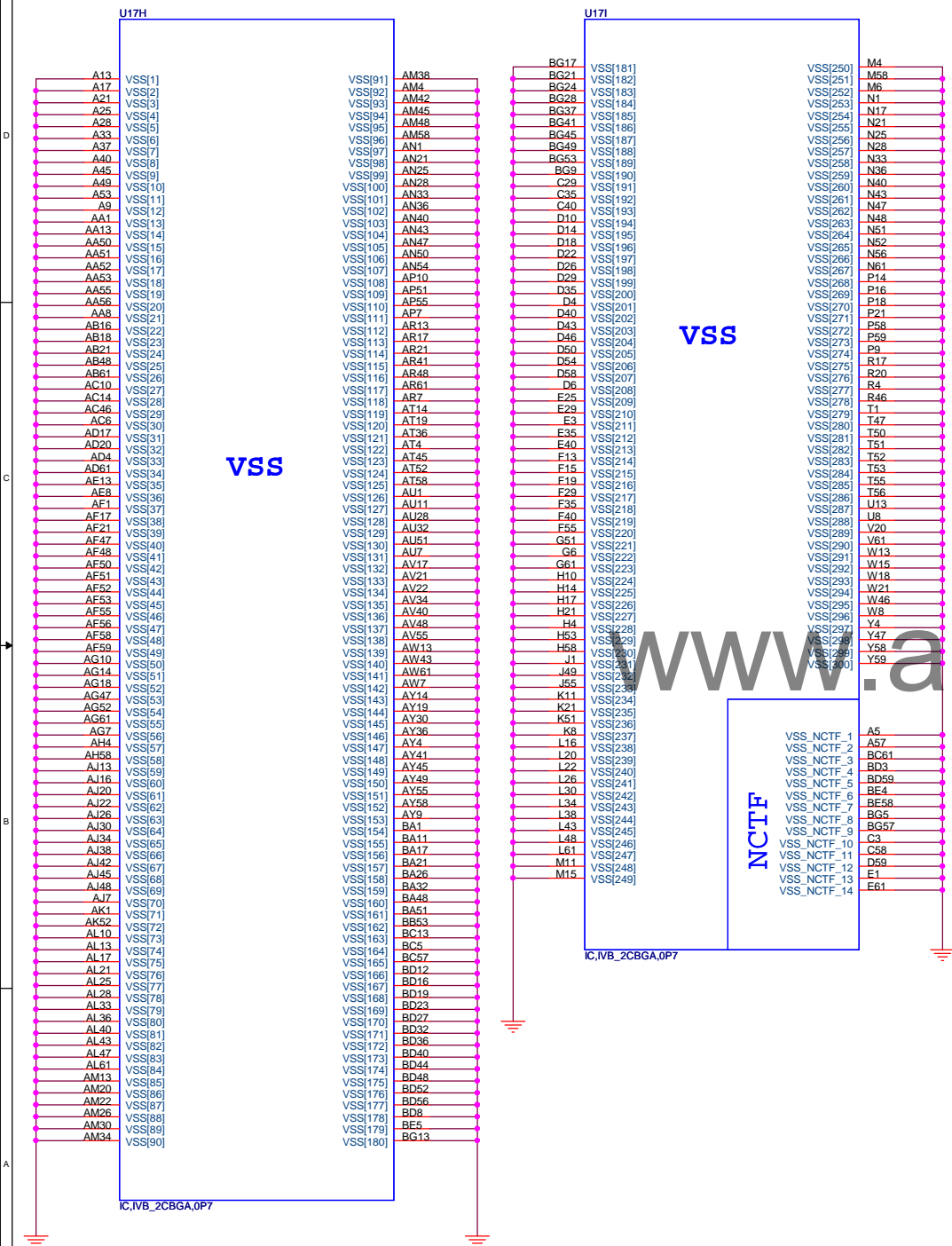
Take care Q3  $V_{gs}(\text{MAX})=2.5$



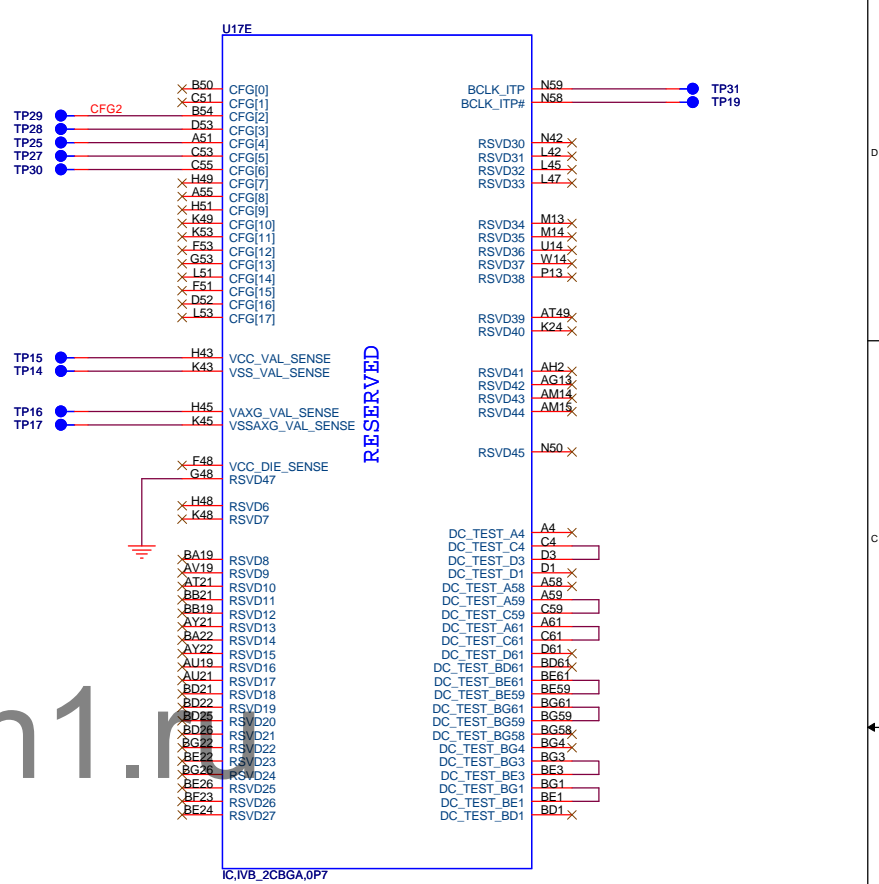
PROJECT : V07

Size	Document Number	Re
<b>Ivy Bridge 4/5</b>		
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## Ivy Bridge Processor (GND)



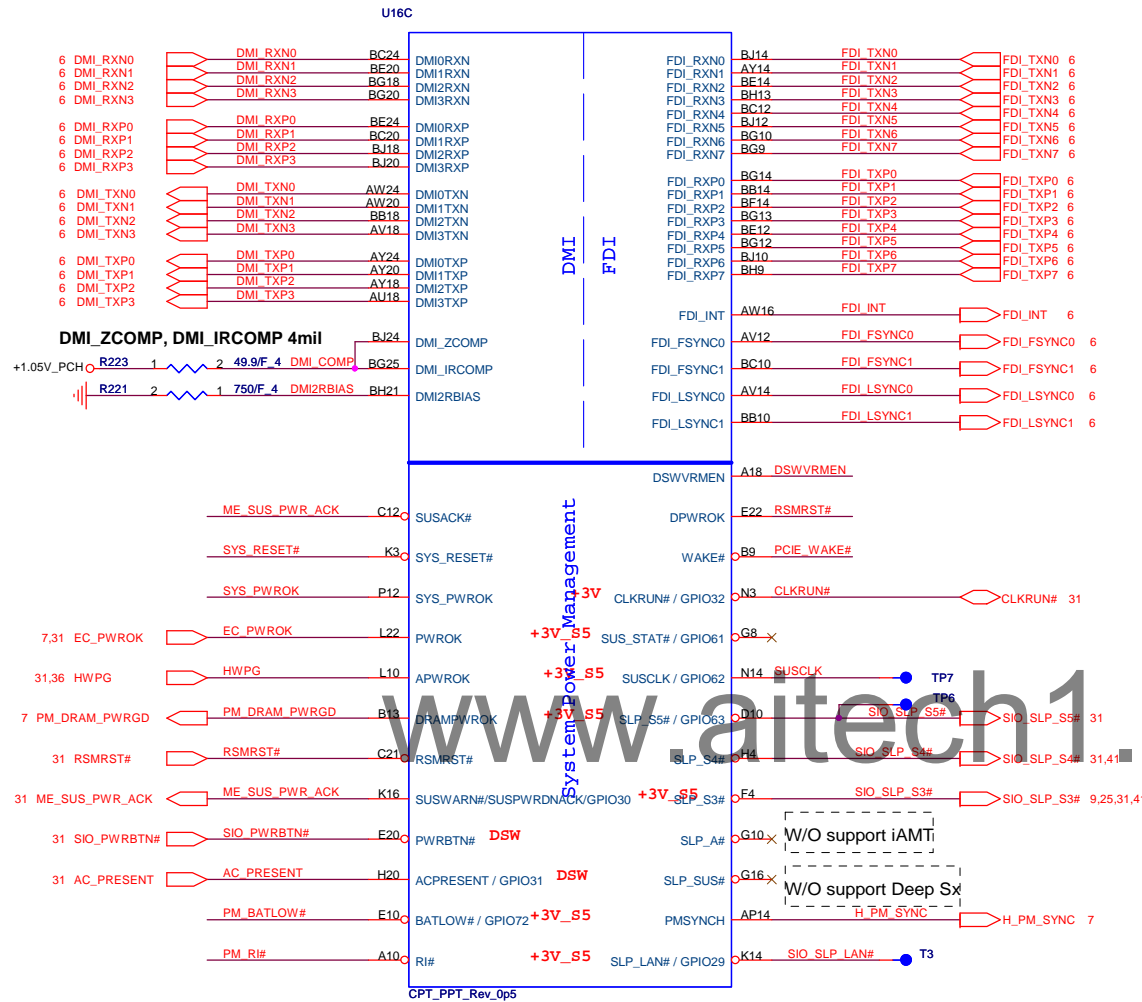
## Ivy Bridge Processor (RESERVED, CFG)



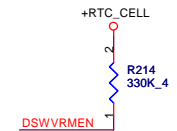
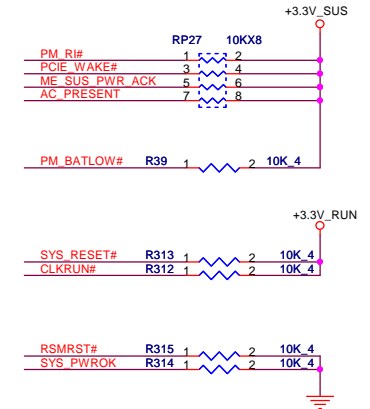




# Cougar Point/Panther Point (DMI,FDI,PM)



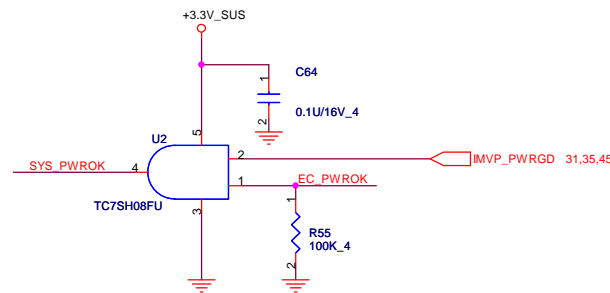
## PCH Pull-high/low(CLG)



On Die DSW VR Enable

High = Enable (Default)

Low = Disable



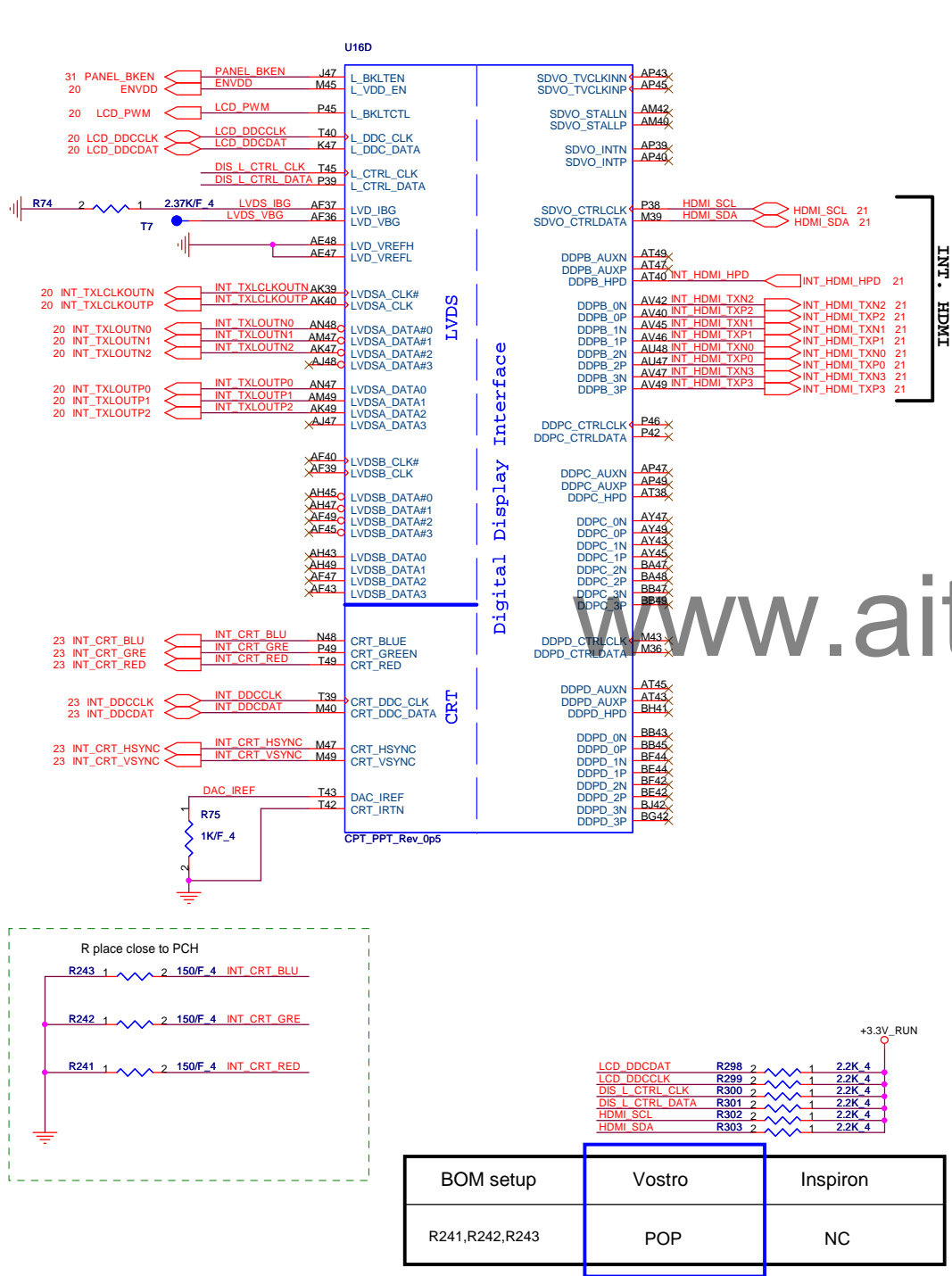
**Quanta Computer Inc.**

**PROJECT : V07**

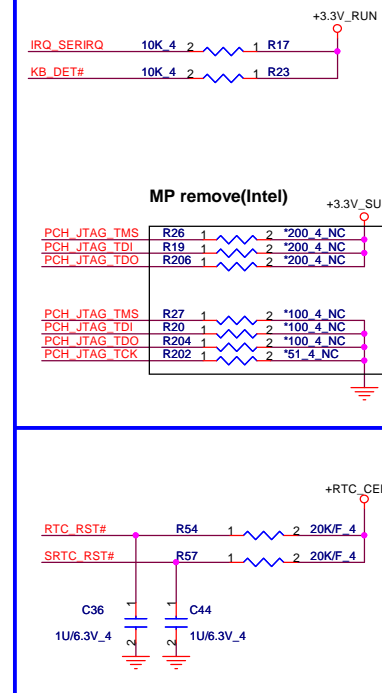
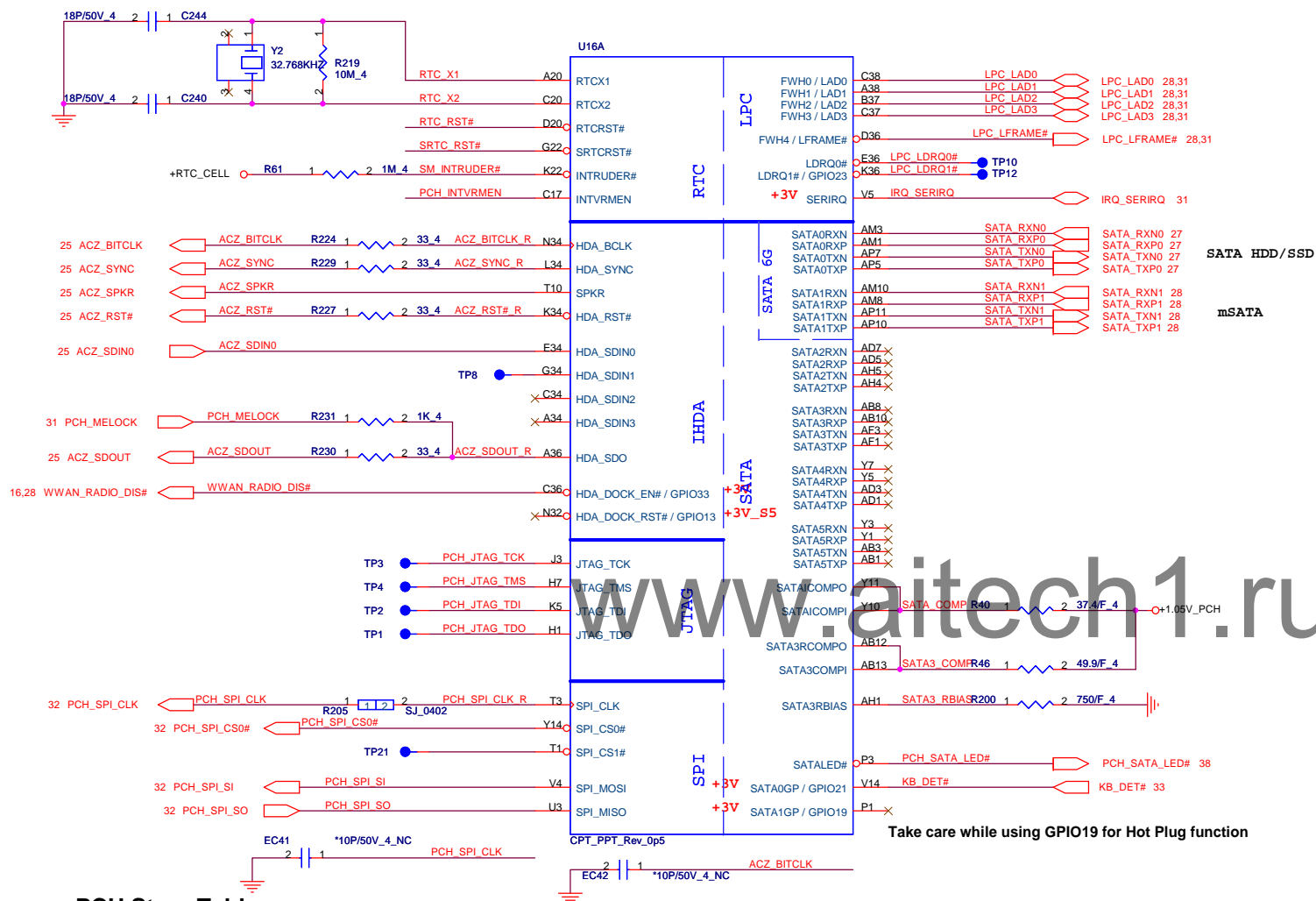


# Cougar Point/Panther Point (LVDS,DDI)

# Cougar Point/Panther Point (GND)



# Cougar Point/Panther Point (HDA,JTAG,SATA)

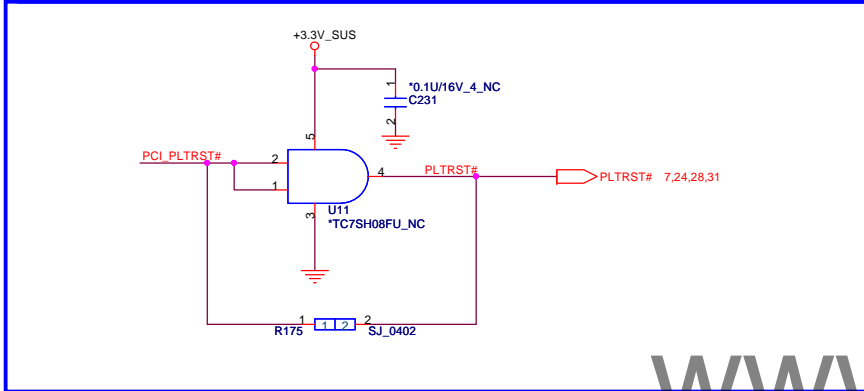
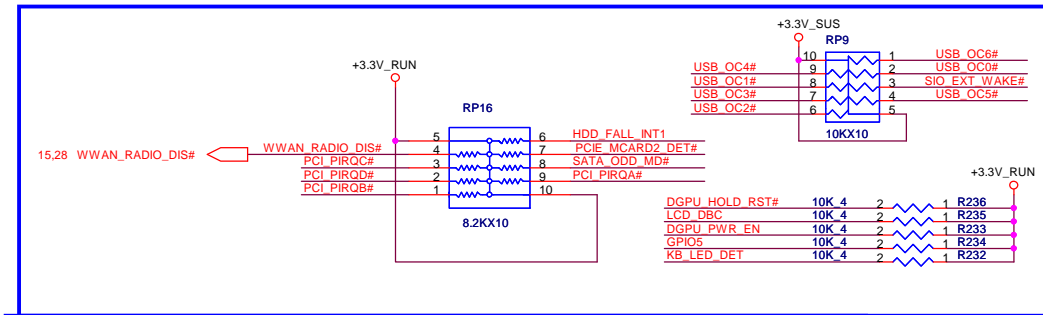


Take care while using GPIO19 for Hot Plug function

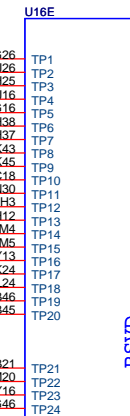
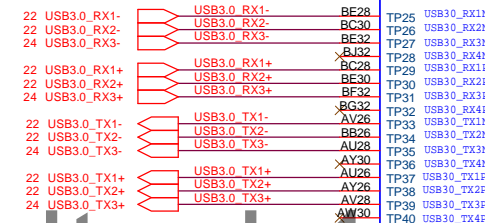
PCH Strap Table

Pin Name	Strap description	Sampled	Configuration	note
SPKR	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode	
HDA_SDO	Flash Descriptor Security	PWROK	0 = Default (weak pull-down 20K) 1 = Override	
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up	+RTC_CELL R215 1 2 330K 4 PCH_INTVRMEN
HDA_SYNC	On-Die PLL VR Volatge Select	RSMRST	0 = Support by 1.8V (weak PD) 1 = Support by 1.5V	+3.3V_SUS R67 1 2 1K 4 ACZ_SYNC_R

# Cougar Point-M/Panther Point (PCI,USB,NVRAM)



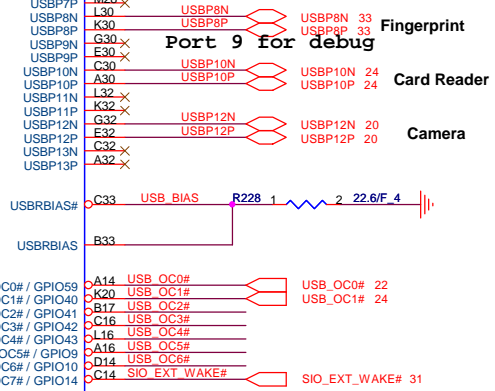
## USB3.0



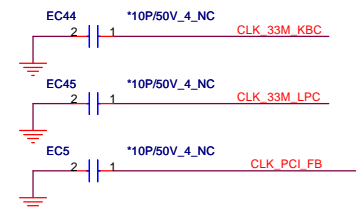
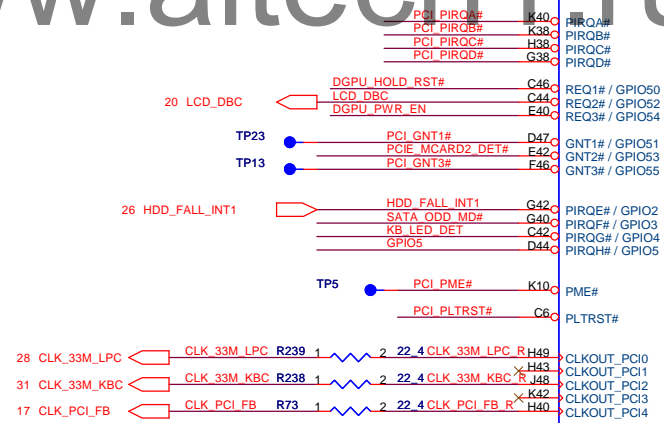
## RSVD

## PCI

## USB



Pin Name	Strap description	Sampled	Configuration									
GNT2# / GPIO53	ESI strap (Server only)	PWROK	Should not be pull-down (weak pull-up 20K)									
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)									
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK	<table><tr><th>Bit 0</th><th>Bit 1</th><th>Boot Location</th></tr><tr><td>1</td><td>1</td><td>SPI *</td></tr><tr><td>0</td><td>0</td><td>LPC</td></tr></table>	Bit 0	Bit 1	Boot Location	1	1	SPI *	0	0	LPC
Bit 0	Bit 1	Boot Location										
1	1	SPI *										
0	0	LPC										
GPIO19	Boot BIOS Selection 0 [bit-0]	PWROK										
Default weak pull-up on GNT0/1# [Need external pull-down for LPC BIOS]												
DF_TV5	DMI and FDI Tx/Rx Termination Voltage	PWROK	weak pull-down 20kohm									

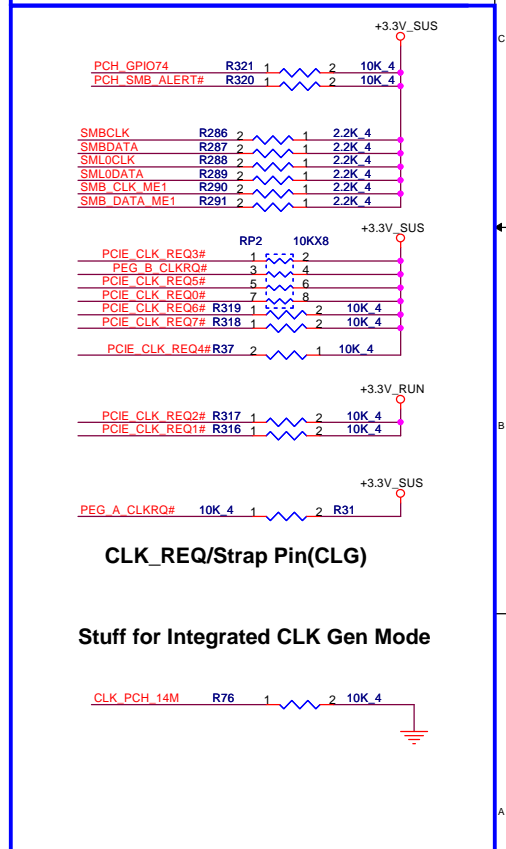
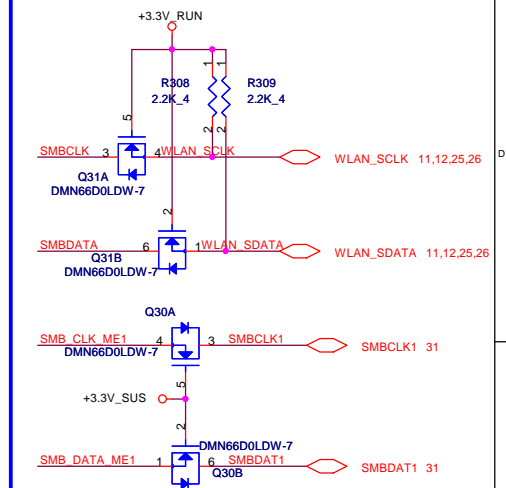




**U16B Cougar Point-M/Panther Point (PCI-E,SMBUS,CLK)**



	Configurable as a GPIO or as a programmable output clock which can be configured as one of the following:
CLKOUTFLEX0 / GPIO64	• 33 / 27 / 48/ 14.318 MHz / DC Output logic '0'
CLKOUTFLEX1 / GPIO65	unsupported clock output value (Default) / 27/ 14.318 MHz output to SIO/EC / 48/24 MHz
CLKOUTFLEX2 / GPIO66	• 33/25/27/48/24/14.318 MHz / DC Output logic '0'
CLKOUTFLEX3 / GPIO67	• 27/14.318 output to SIO/48/24 MHz (Default)



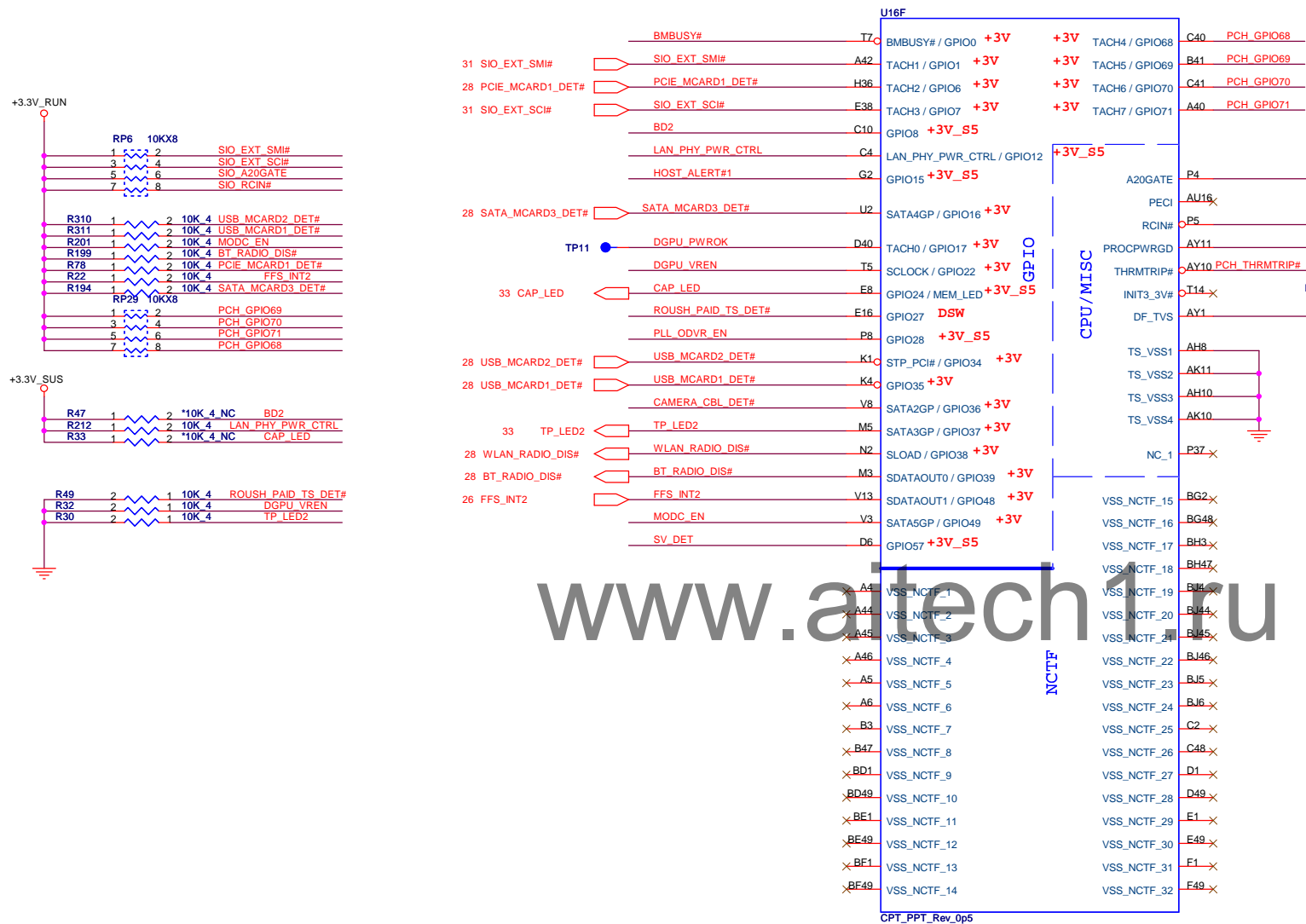
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**PROJECT : V07**

**Panther Point 5/7**

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# Cougar Point/Panther Point (GPIO,VSS\_NCTF,RSVD)



Pin Name	Strap description	Sampled	Configuration
GPIO28	On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (Default)

	DMI TERMINATION VOLTAGE OVERRIDE  Low = Tx, Rx terminated to same voltage (DC Coupling Mode) (DEFAULT)
--	---

## SGPIO



BMBUSY#:(Intel feedback)  
Follow CRB checklist, 1K is  
for intel BIOS validation purpose.

BMBUSY#:  
If not used, require a weak pull-up  
(8.2- KΩ to 10 KΩ) to Vcc3\_3.  
CRB(V1.0)P28: it has 1K PU and  
100 ohm on this net for validation purpose.

Intel ME Crypto Transport Layer Security (TLS) cipher suite  Low = Disable (Default) High = Enable	

## MFG-TEST

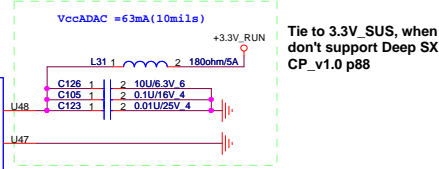
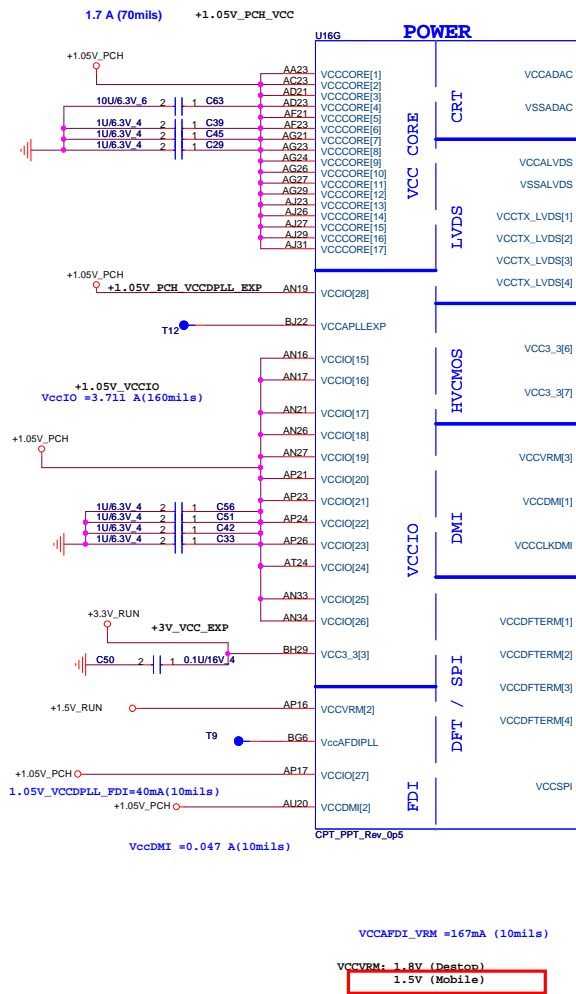


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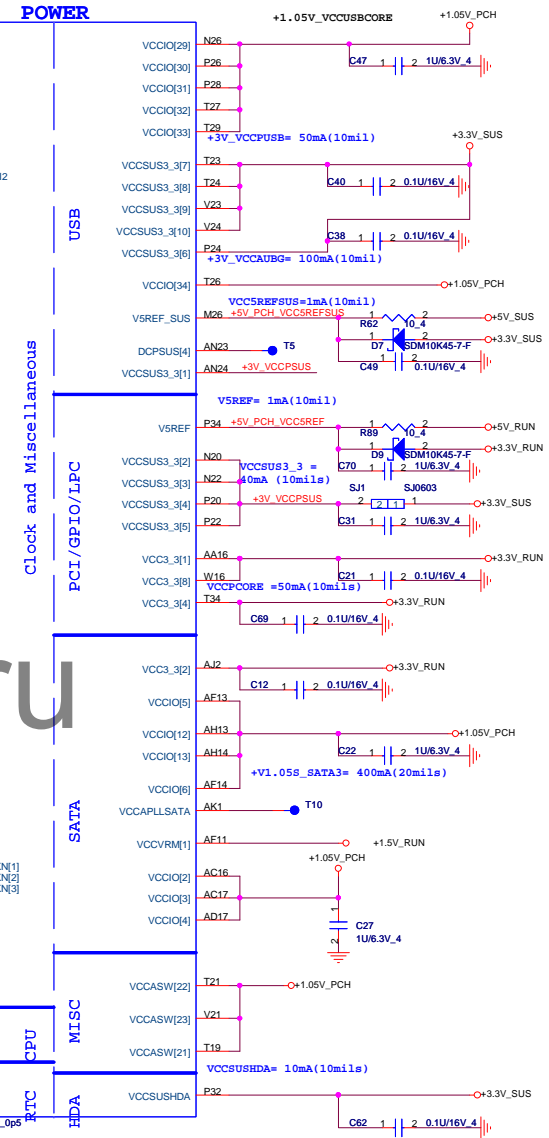
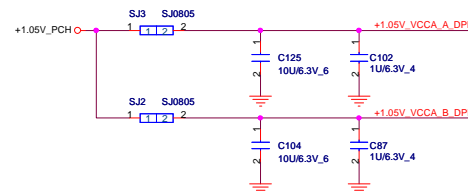
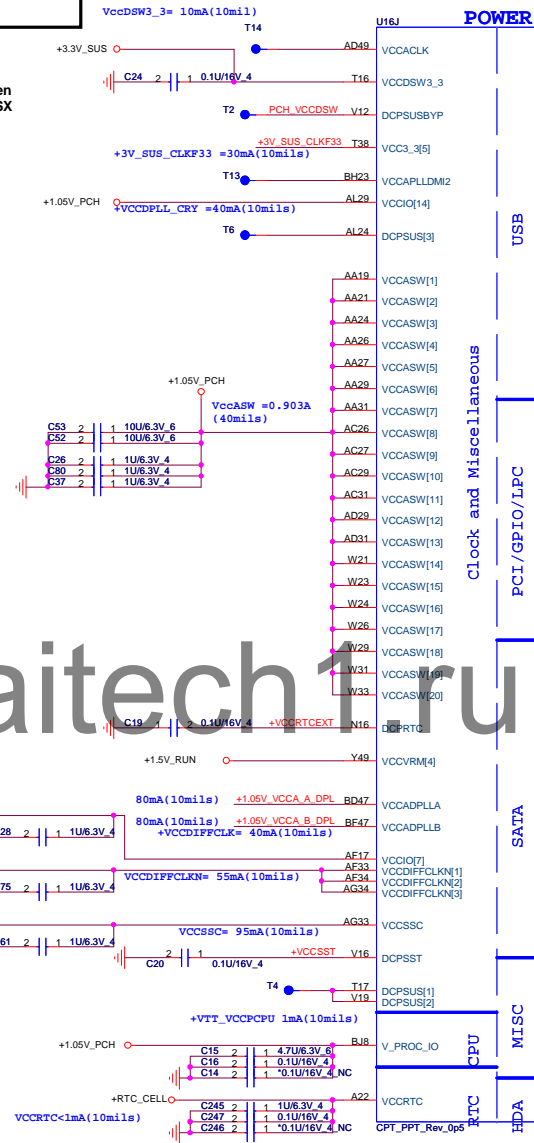
Size	Document Number	Rev
	<b>Panther Point 6/7</b>	1A
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BOM setup	VOSTOR(V07)	Inspiron(R07)
L31 QPN	CX000181024	CS00003J951

BOM setup	VOSTOR(V07)	Inspiron(R07)
C126,C105 C123	POP	NC

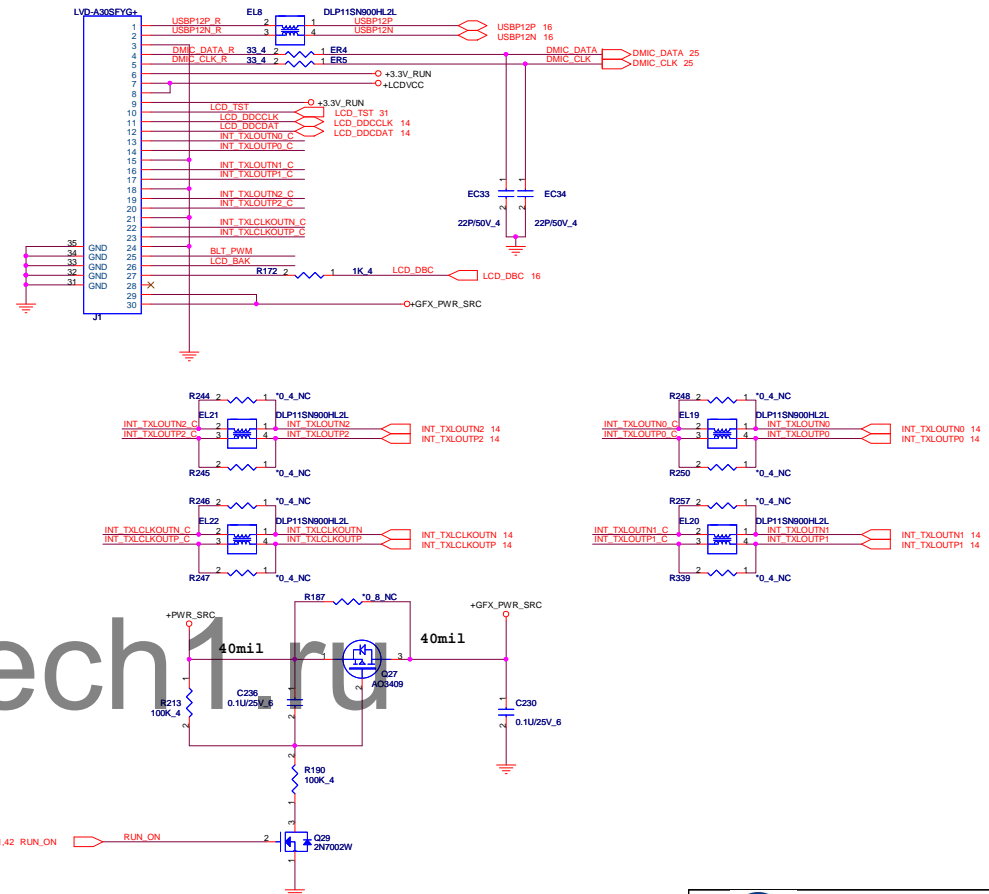
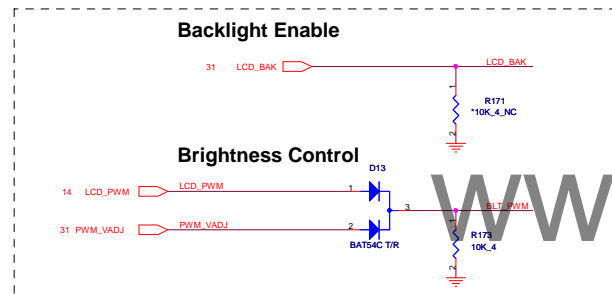
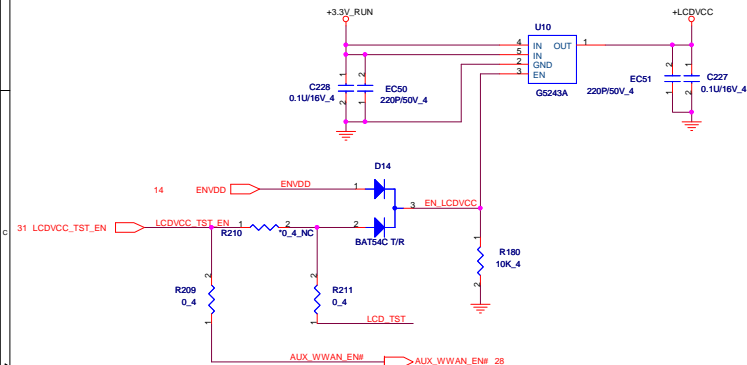


**Tie to 3.3V\_SUS, when  
don't support Deep SX  
CP\_v1.0 p88**

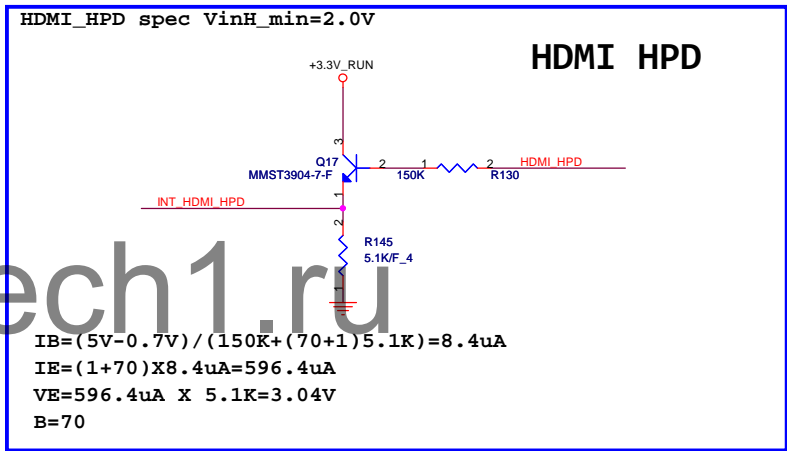


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**PROJECT :V07**

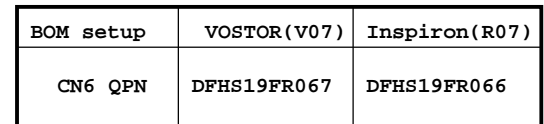
Size	Document Number <b>Panther Point 7/7</b>	Rev 1A
Date:	Monday, January 09, 2012	Sheet 19 of 46



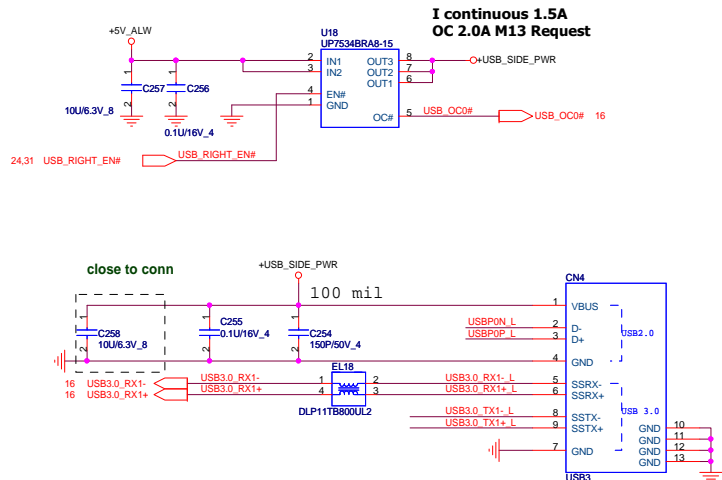
## Reserve for EMI and close to HDMI CONN



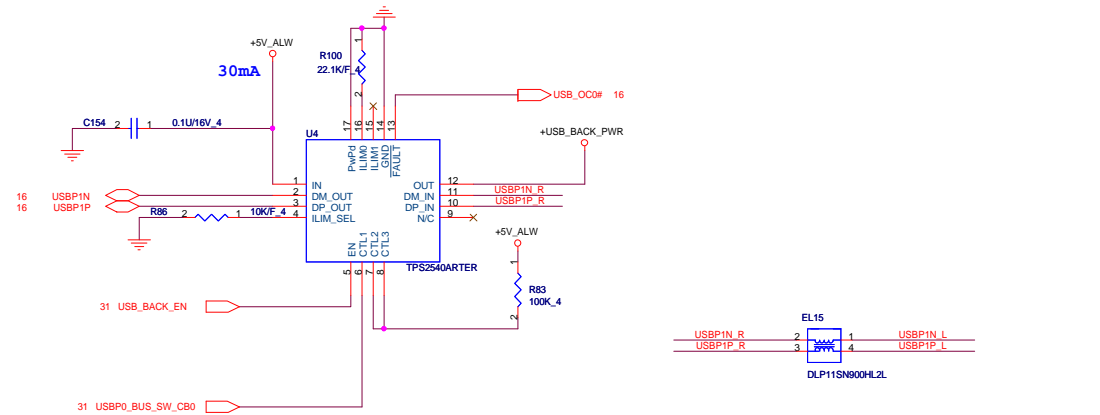
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## USB3.0 x2 (x1 with powershare)



## S3/S5 USB charging circuit



USBP0_BUS_SW_CB0	Mode
Low	DCP, Auto-detect
High	CDP, BC Spec 1.1

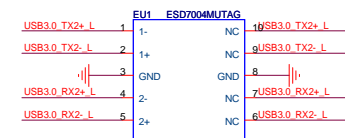
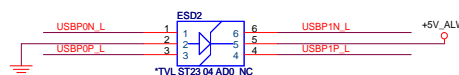
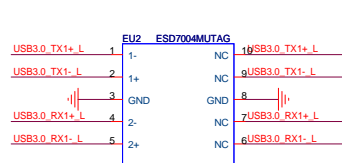
OC limitation	R8224	mA
	100k ohm	480
	22.1k ohm	2171

Applied Now

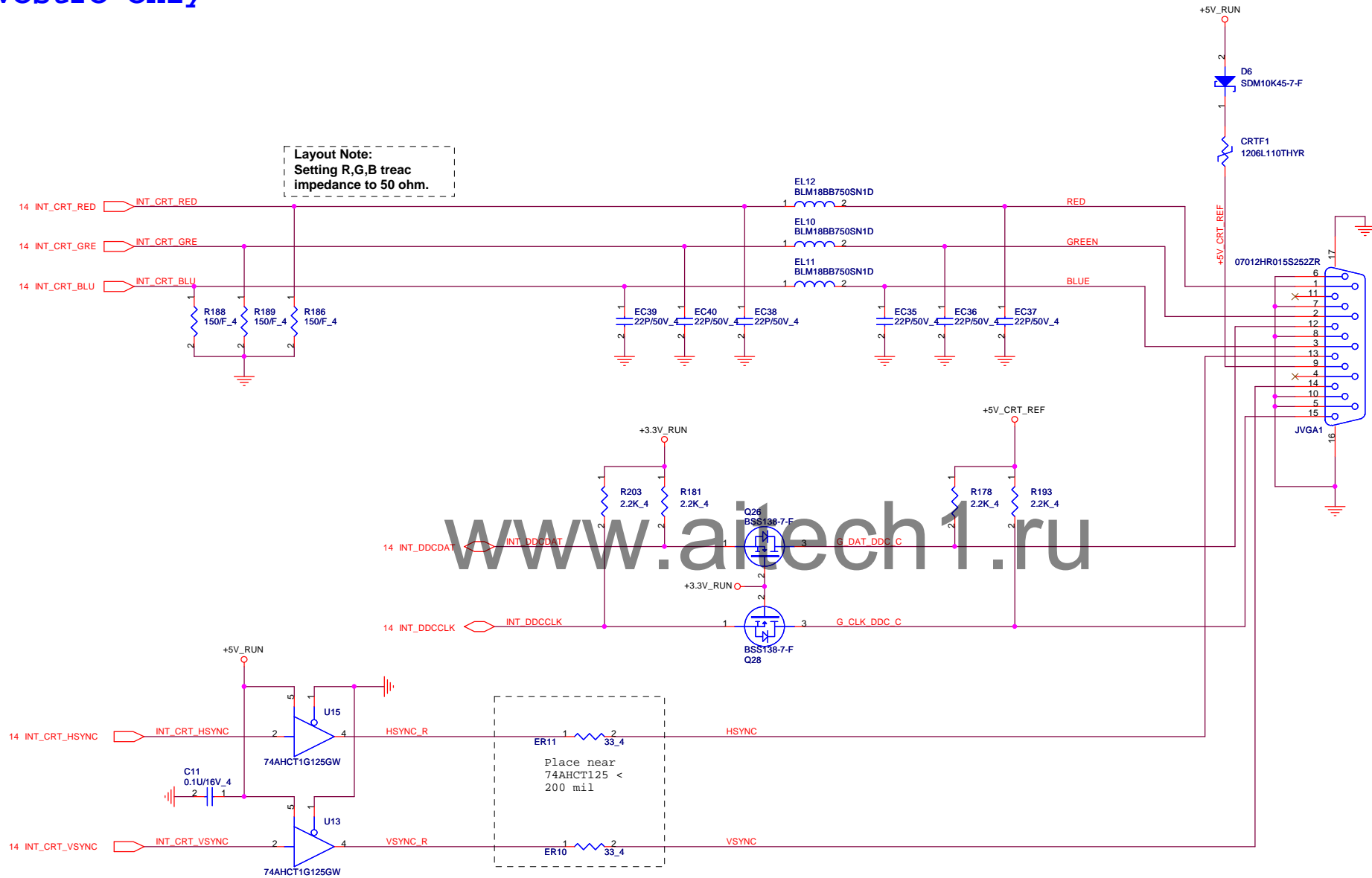
www.aitech1.ru

## ESD Function

Place ESD diodes as close as USB connector.

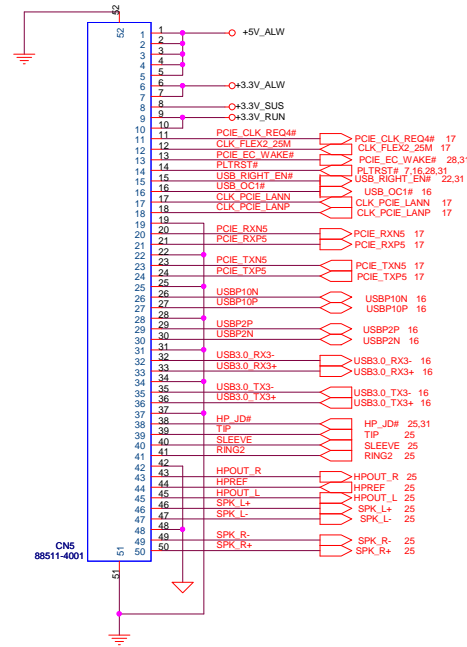
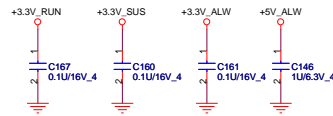


# Vostro only



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**PROJECT : V07**

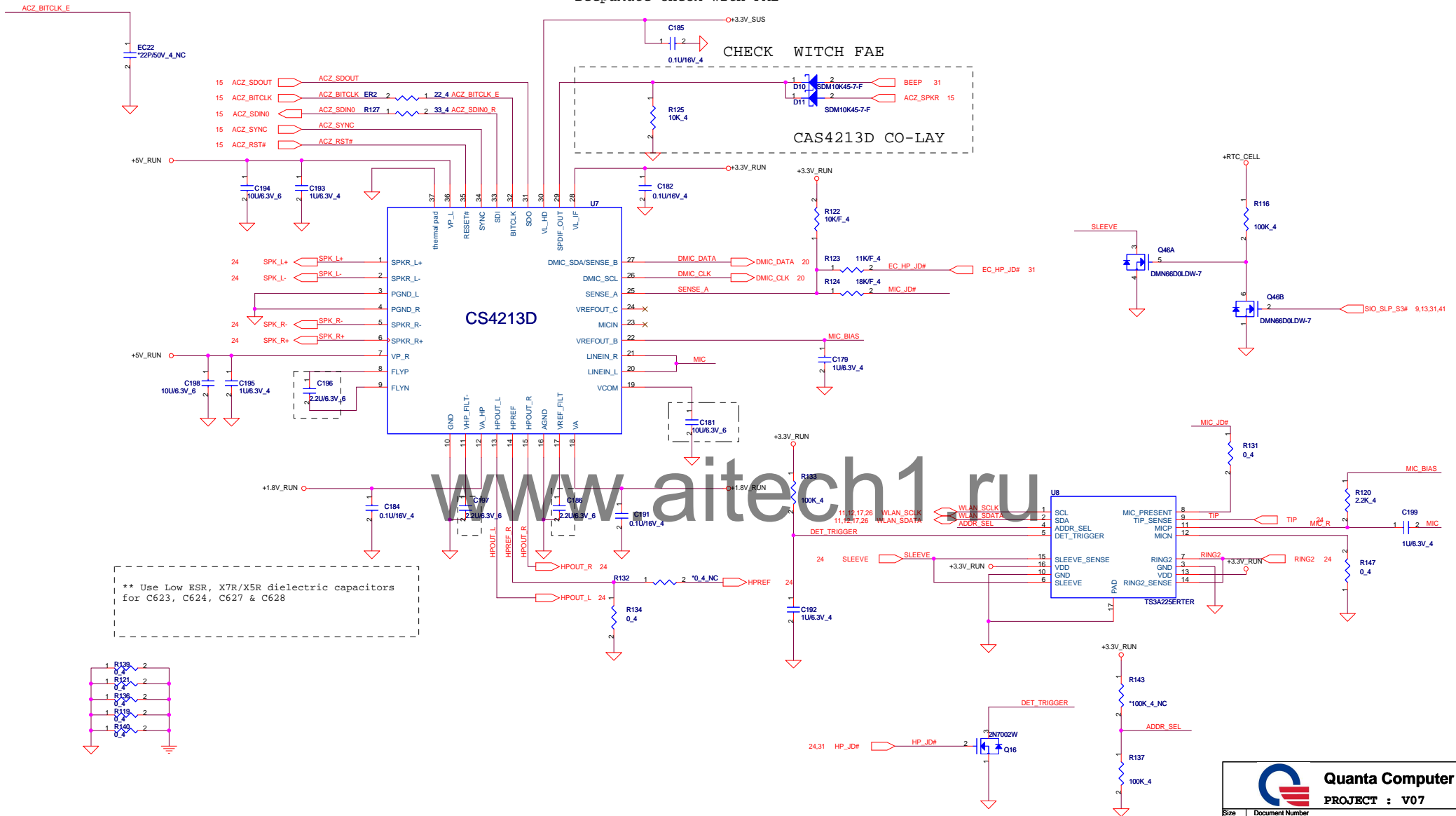
Size	Document Number	Rev
	VGA	1A
Date:	Monday, January 09, 2012	Sheet 23 of 46



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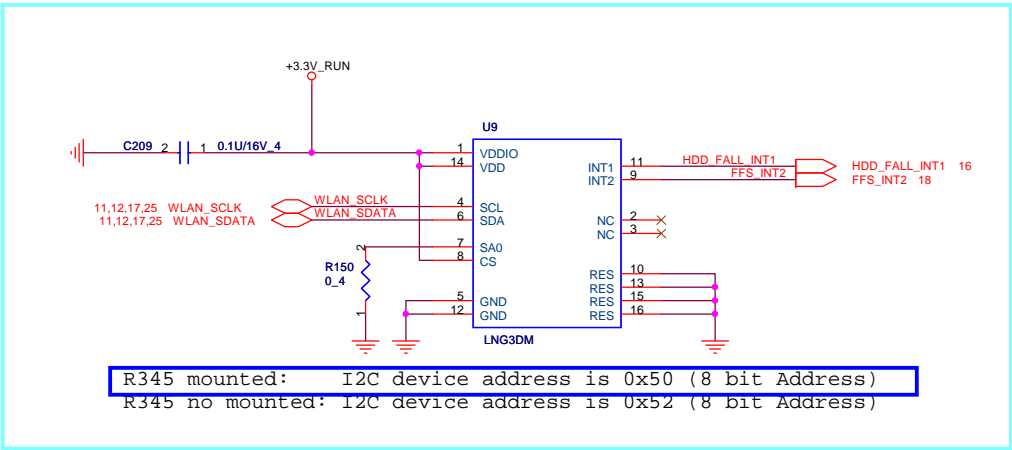
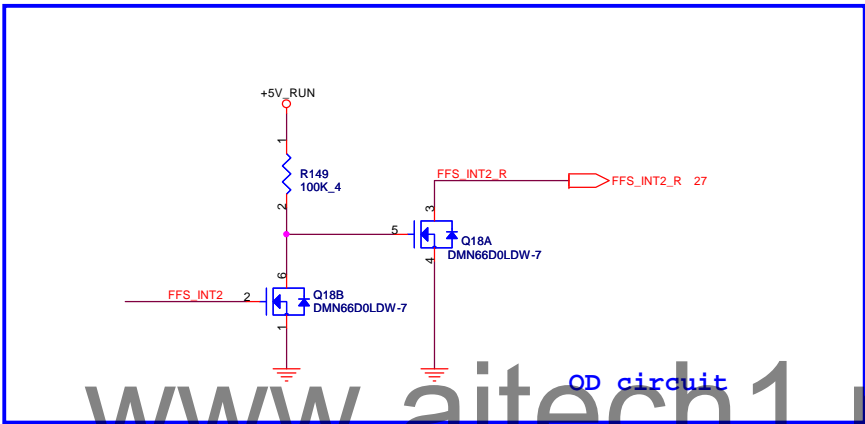
# Beep&Mute check with FAE



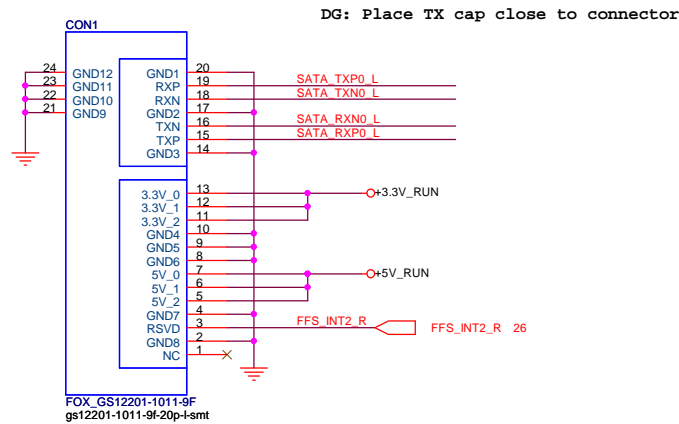
# 3-axis Fall Sensor

Vostro only

If you have two HDD,need add two OD circuit for Fall sensor interrupt circuit

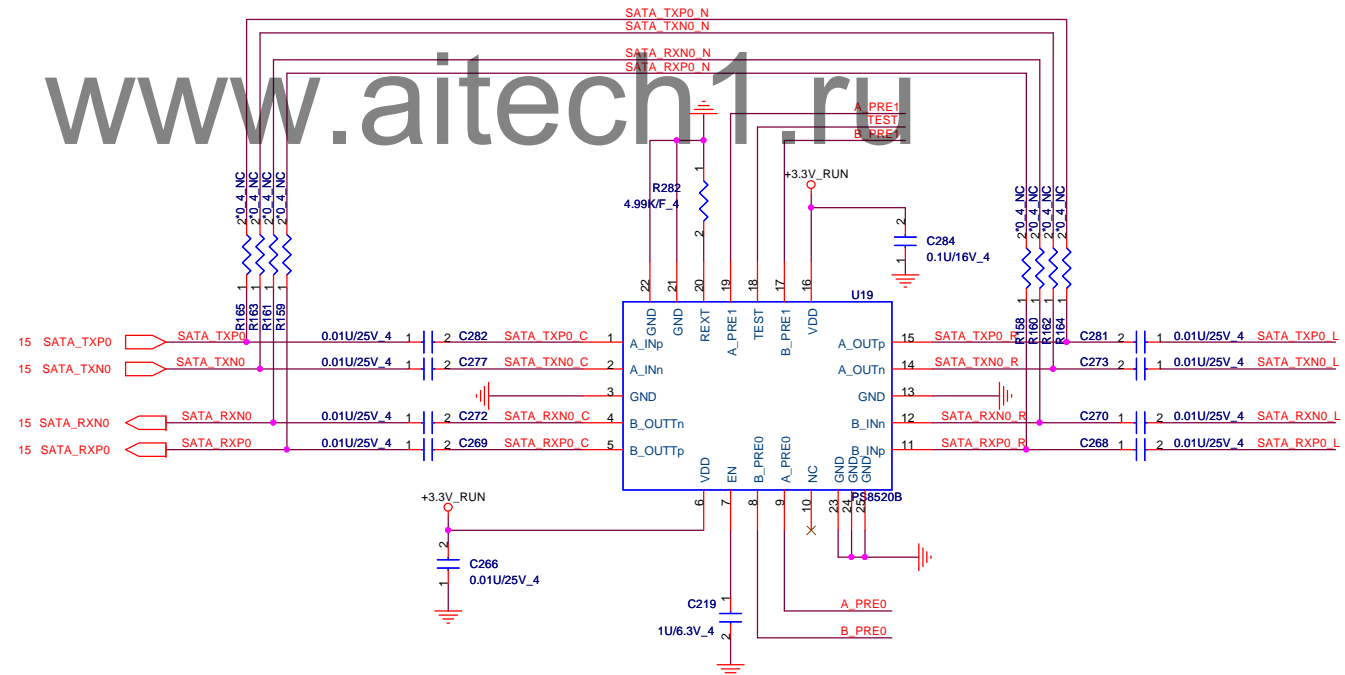
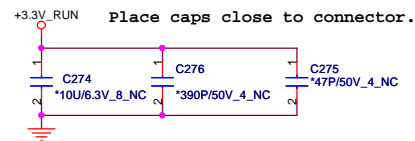
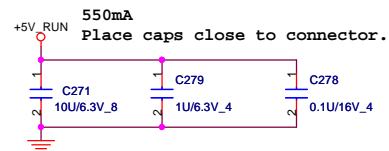


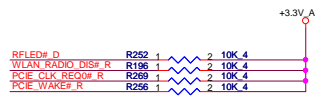
## HDD



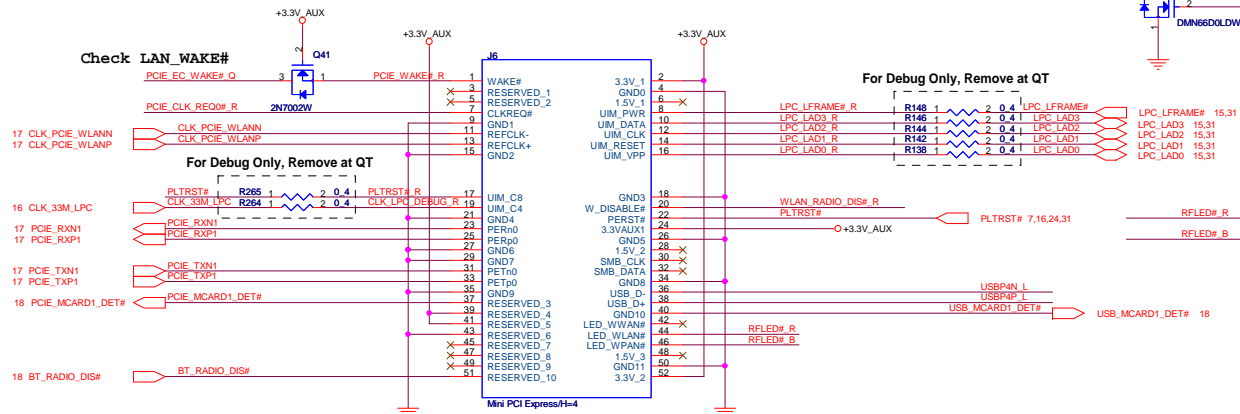
A_PRE0	A_PRE1	SATA TX Emphasis
0	0	0db
0	1	1.5db
1	0	2.5db
1	1	3db

B_PRE0	B_PRE1	SATA RX Emphasis
0	0	0db
0	1	1.5db
1	0	2.5db
1	1	3db

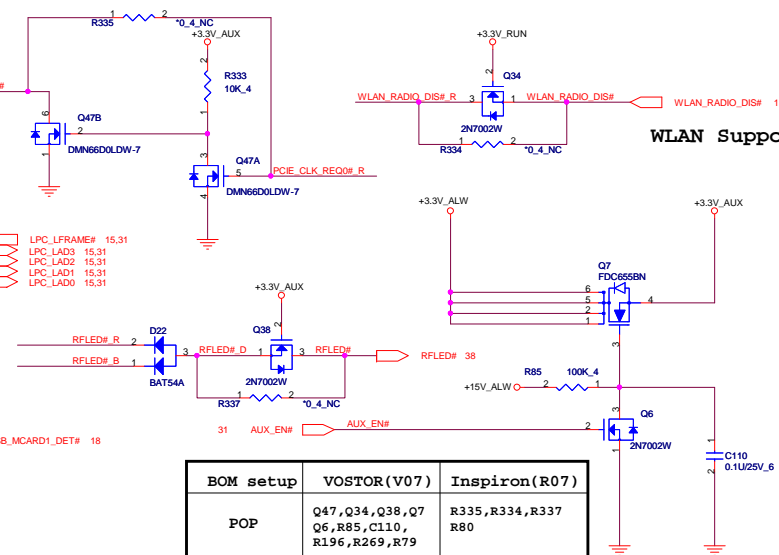




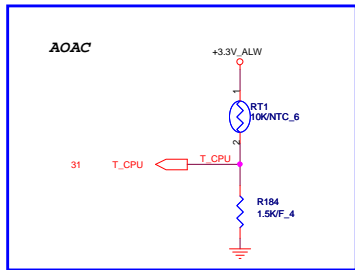
## MiniCard WLAN connector



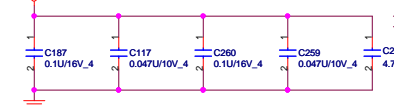
## WLAN Support AOAC



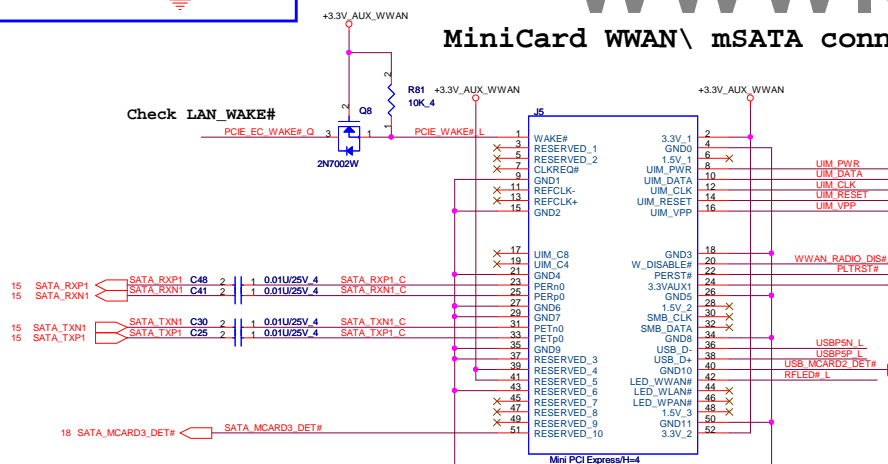
BOM setup	VOSTOR(V07)	Inspiron(R07)
POP	Q47, Q34, Q38, Q7 Q6, R85, C110, R196, R269, R79	R335, R334, R337 R80
NC	R335, R334, R337 R80	Q47, Q34, Q38, Q7 Q6, R85, C110, R196 R269, R79



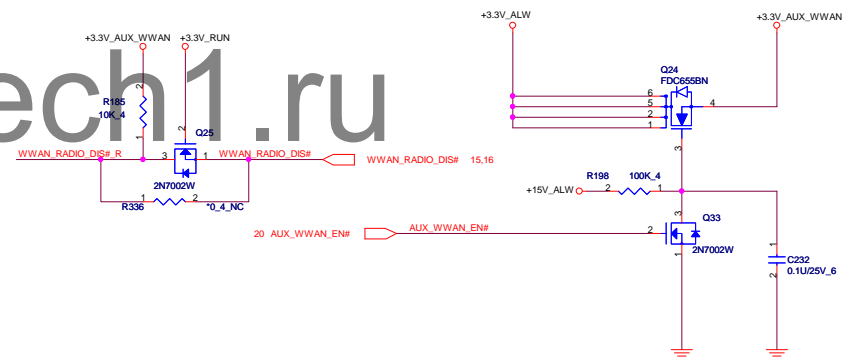
Place caps close to connector.



## MiniCard WWAN\ mSATA connector

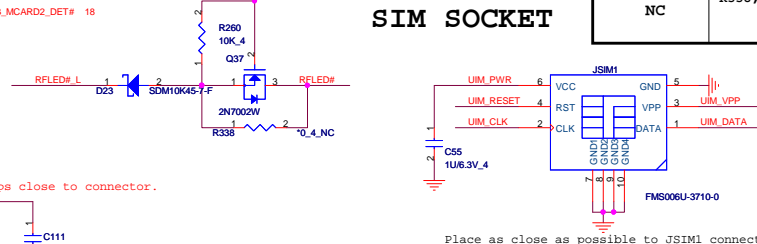


## WWAN Support AOAC



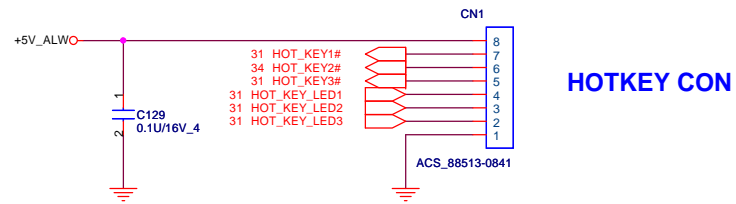
BOM setup	VOSTOR(V07)	Inspiron(R07)
POP	Q37, Q25, Q24, Q33 , R198, C232, R185	R338, R336
NC	R338, R336	Q37, Q25, Q24, Q33 , R198, C232, R185

## SIM SOCKET



Place as close as possible to JSIM1 connector

Spacing 2:1




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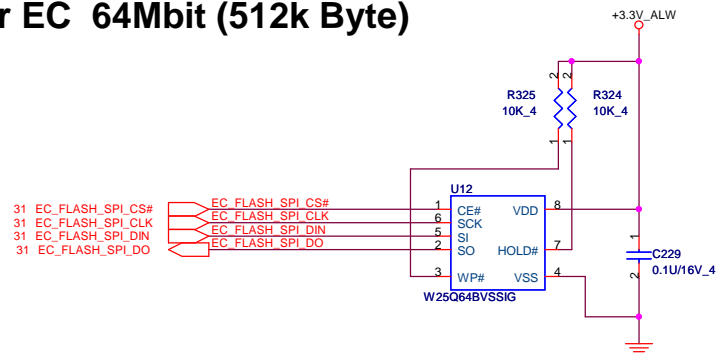
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		<b>Quanta Computer Inc.</b>	
		<b>PROJECT : v07</b>	
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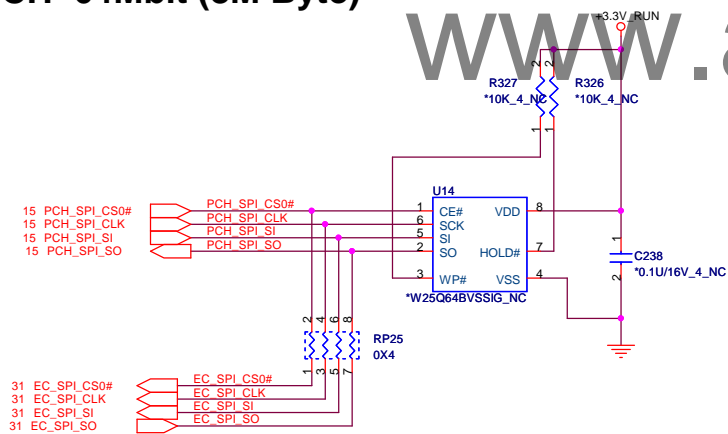


## FLASH / RTC

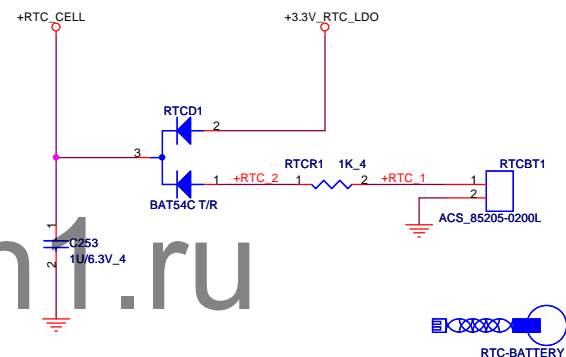
### For EC 64Mbit (512k Byte)



### For PCH 64Mbit (8M Byte)



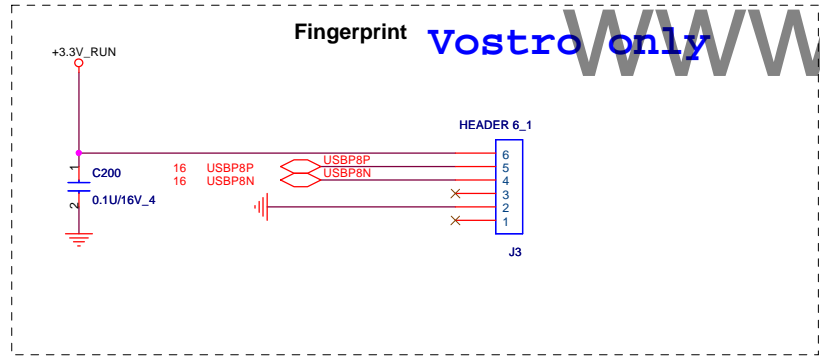
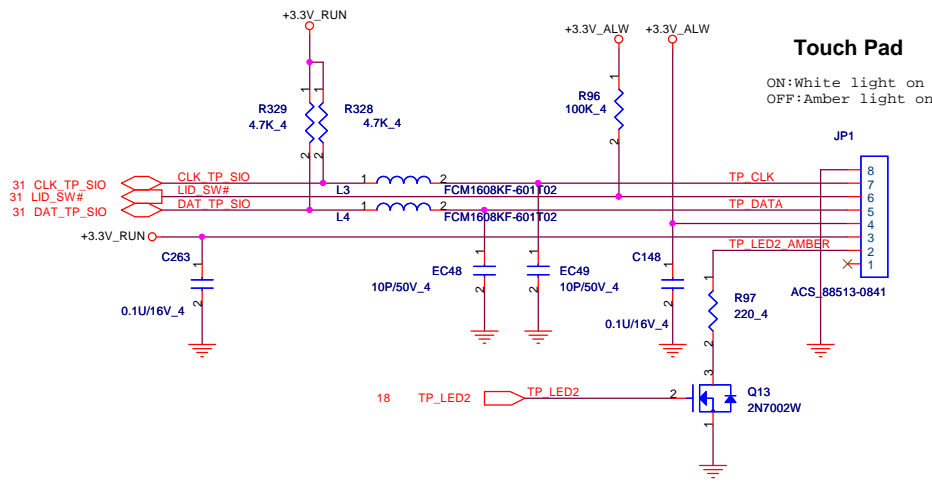
## RTC



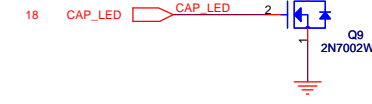
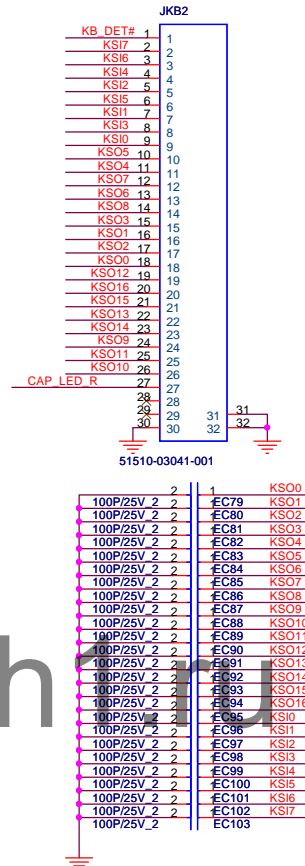
Double, 25'C, Vf=0.4V, If=25mA  
one, 25'C, Vf=0.35V, If=15.8mA



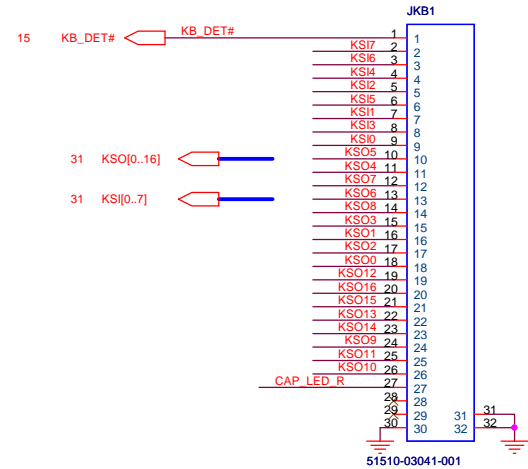
KEYBOARD CONNECTOR



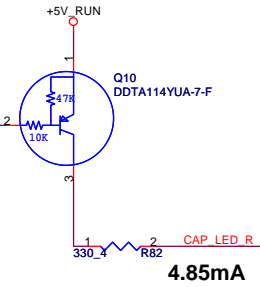
Vostro



Inspiron



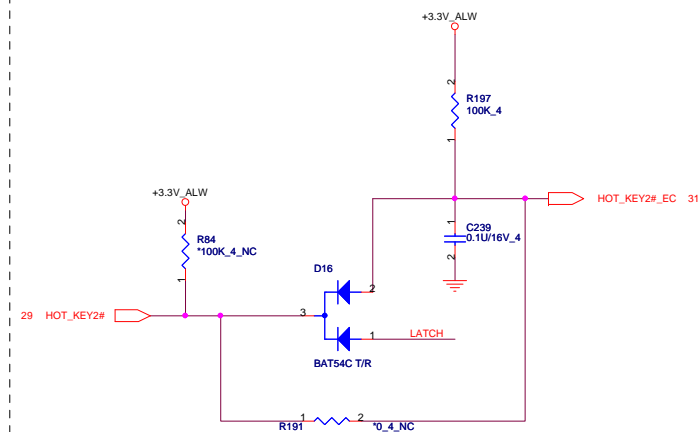
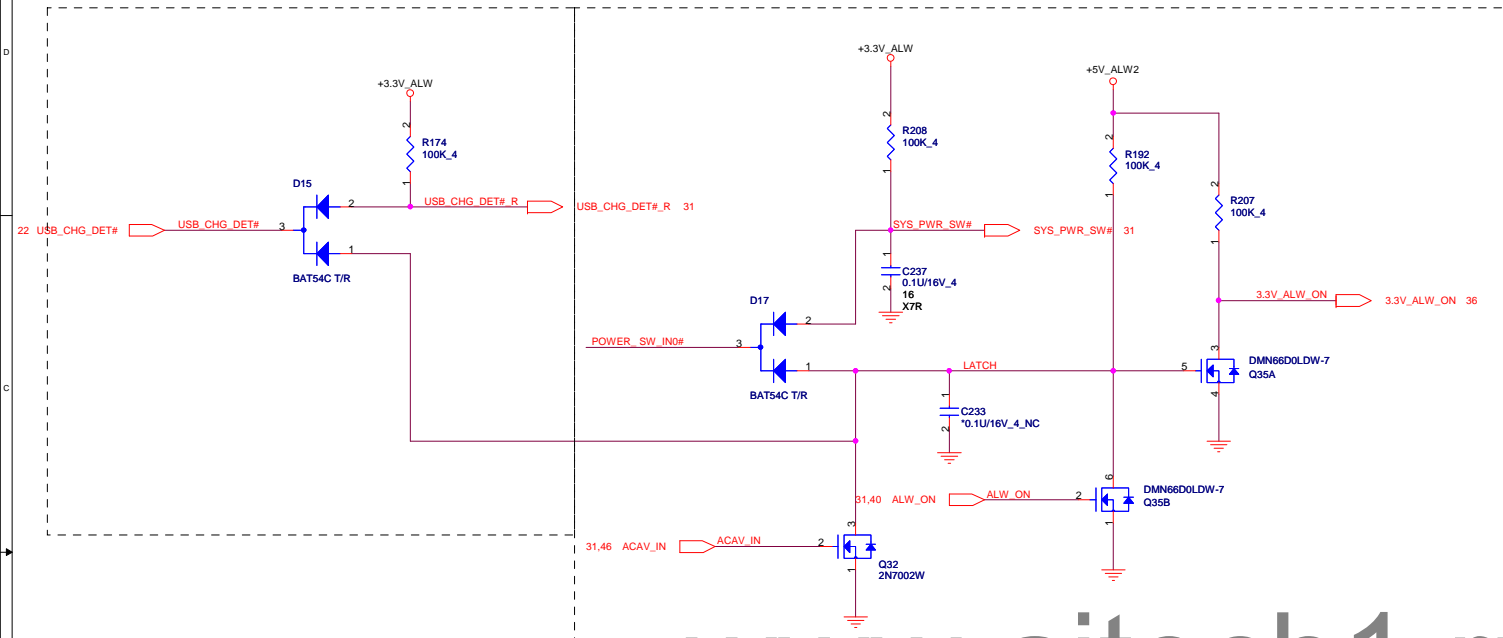
Vi(on\_max)=-1.4V  
Vi(off\_min)=-0.3



## For USB charger usage

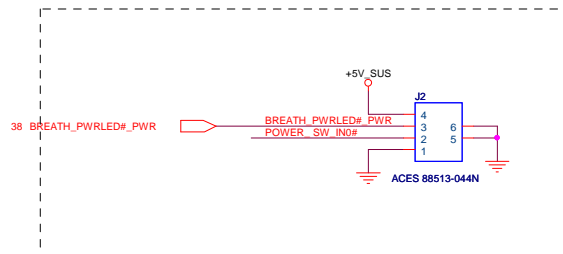
## 3V ALW ON POWER LOGIC

## Instant ON function Vostor only



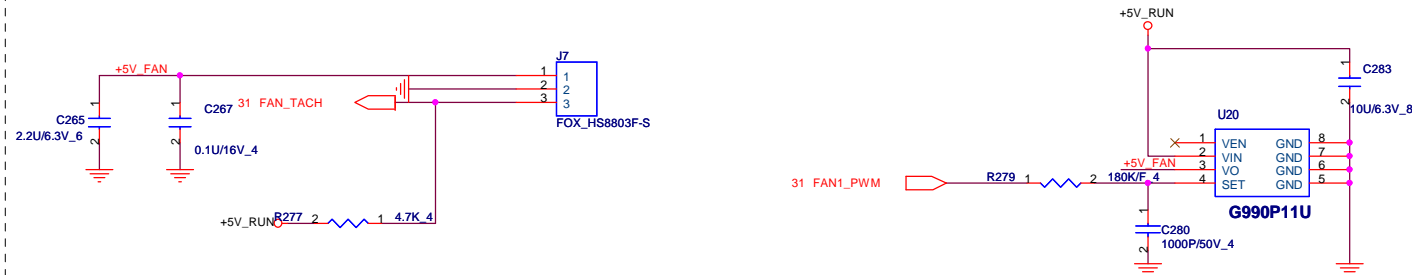
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## TO PWR button board



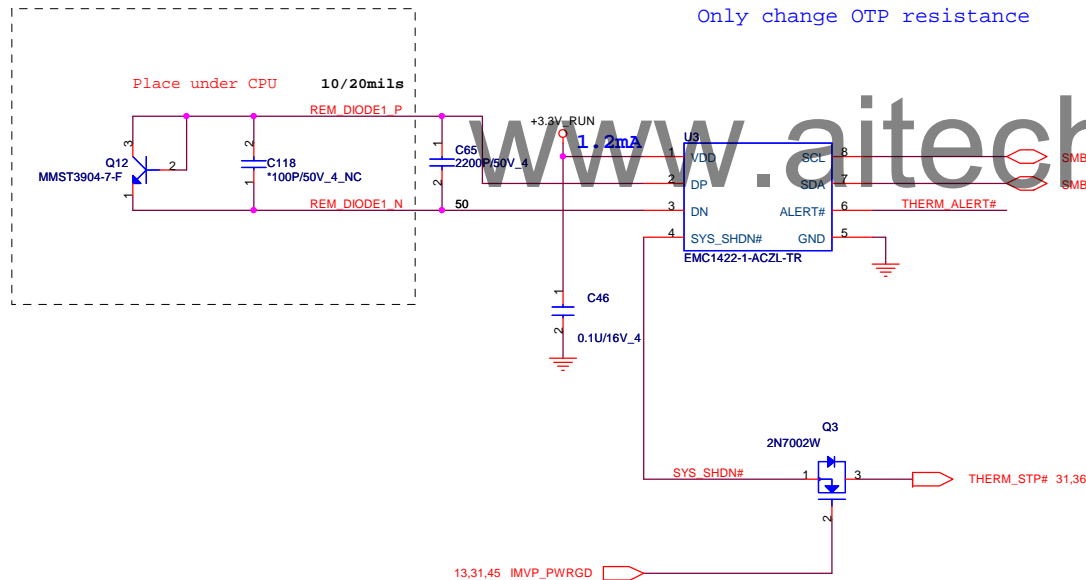
BOM setup	NC	POP
Vostro	R84,R191	D16,C239,R197
Inspiron	D16,C239,R197	R84,R191

## FAN CONTROL



EMC 1422 and NCT7718 PIN TO PIN  
Only change OTP resistance

OTP 85 degree C

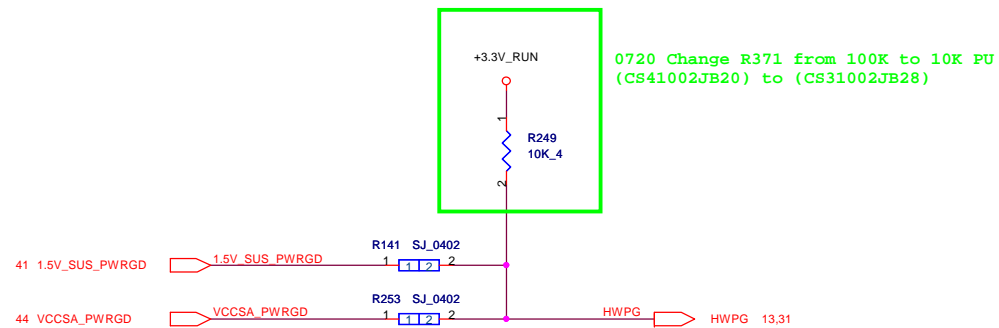


SYS_SHDN#	4.7K	6.8K	10K	15K	22K	33K
ALERT#	4.7K	6.8K	10K	15K	22K	33K
4.7K	77°C	83°C	89°C	95°C	101°C	107°C
6.8K	78°C	84°C	90°C	96°C	102°C	108°C
10K	79°C	85°C	91°C	97°C	103°C	109°C
15K	80°C	86°C	92°C	98°C	104°C	110°C
22K	81°C	87°C	93°C	99°C	105°C	111°C
33K	82°C	88°C	94°C	100°C	106°C	112°C

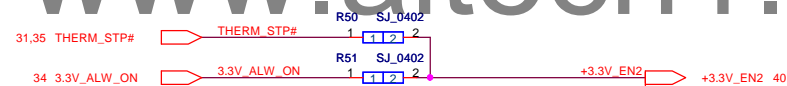


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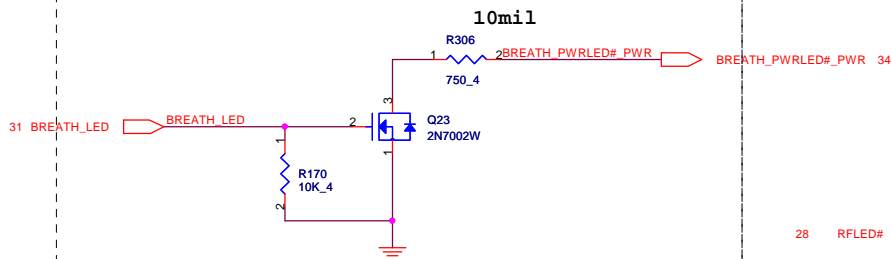


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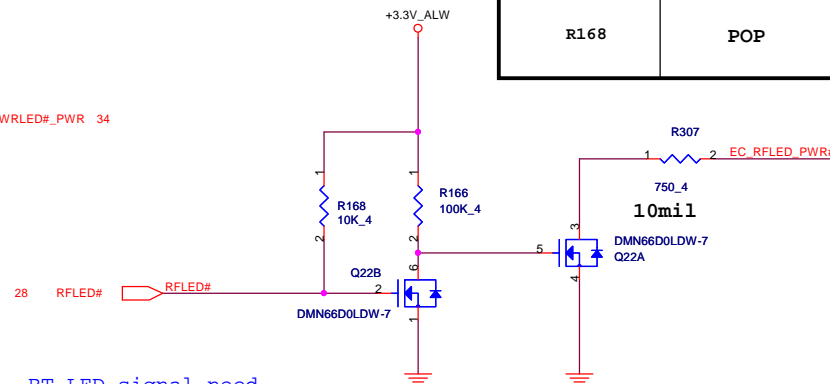
**PROJECT : V07**

Size	Document Number	Rev
	<b>MiniCard / mSATA</b>	<b>1A</b>
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## Power



## Bluetooth / WLAN on/off LED

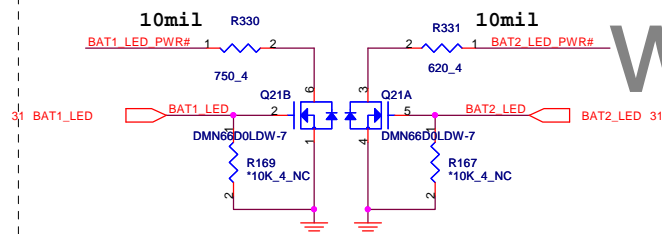


BT LED signal need

Change from 2N7002W-7-F to DMN66D0LDW-7

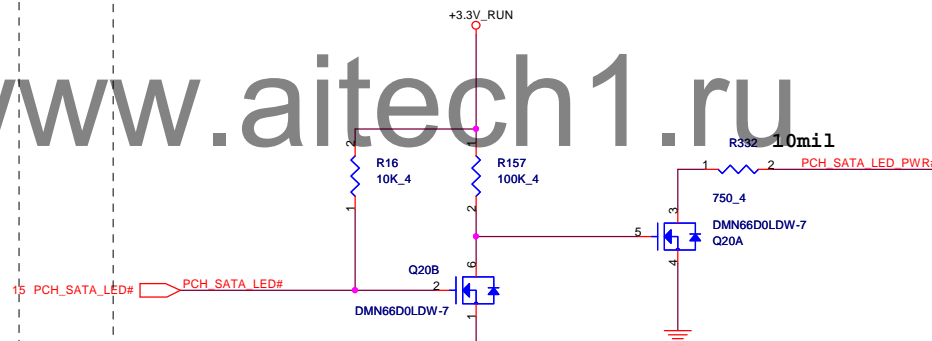
BOM setup	VOSTOR(V07)	Inspiron(R07)
R168	POP	NC

## Battery

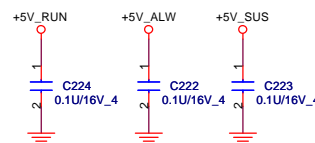
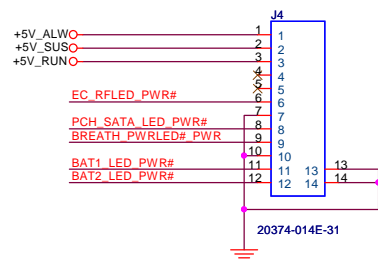


Change from 2N7002W-7-F to DMN66D0LDW-7(9/2)

## HDD activity LED.

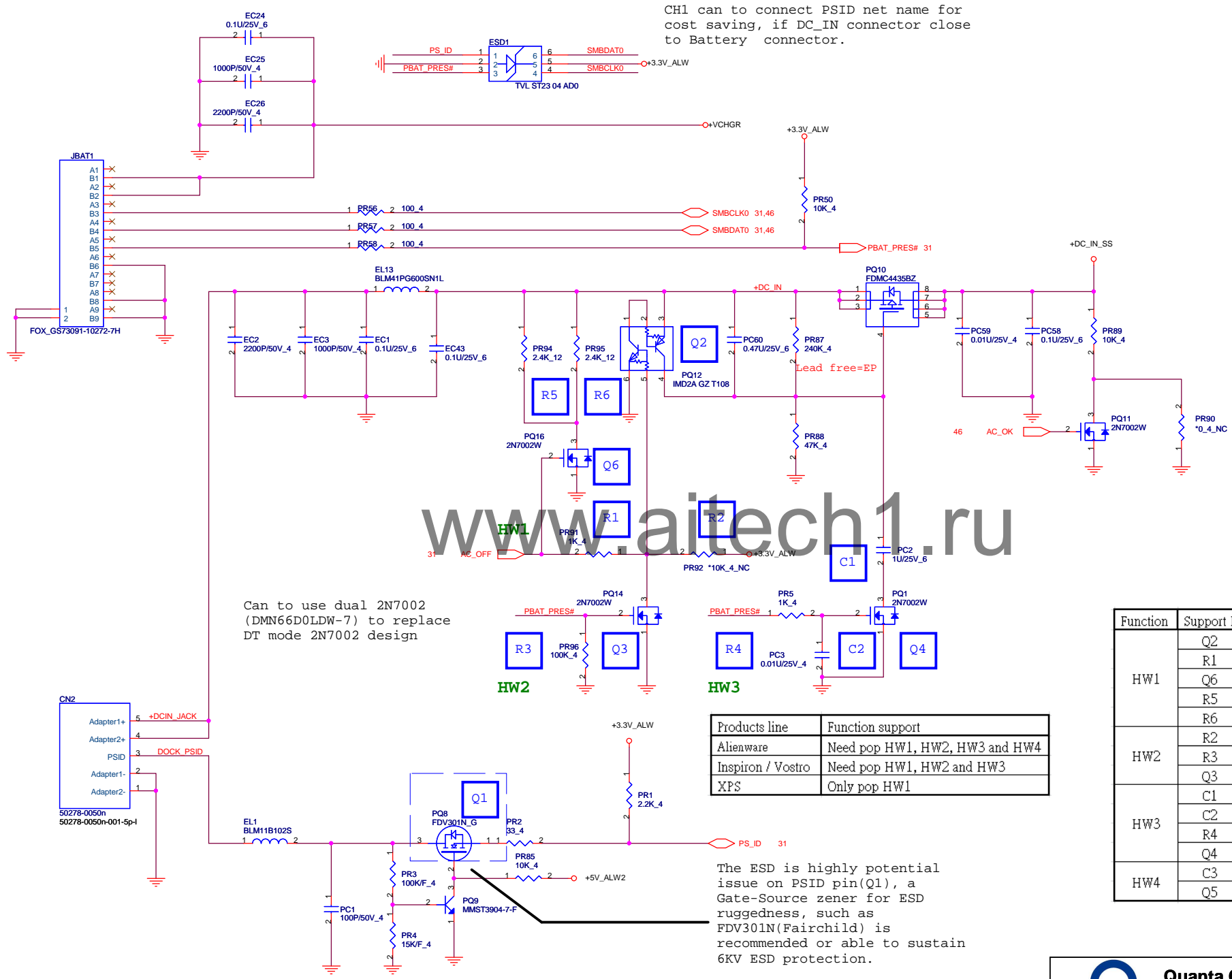


Change from 2N7002W-7-F to DMN66D0LDW-7(9/2)



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	LED board CONN	1A
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CH1 can to connect PSID net name for cost saving, if DC\_IN connector close to Battery connector.

Can to use dual 2N7002 (DMN66D0LDW-7) to replace DT mode 2N7002 design

Products line	Function support
Alienware	Need pop HW1, HW2, HW3 and HW4
Inspiron / Vostro	Need pop HW1, HW2 and HW3
XPS	Only pop HW1

Function	Support DT Mode Components	
HW1	Q2	IMD2AT108
	R1	1K_4
	Q6	2N7002W-7-F
	R5	2.2K_12
	R6	2.2K_12
HW2	R2	10K_4
	R3	100K_4
	Q3	2N7002W-7-F
HW3	C1	1U/6.3V_4
	C2	0.01U/25V_4
	R4	1K_4
	Q4	2N7002W-7-F
HW4	C3	1U/6.3V_4
	Q5	2N7002W-7-F

The ESD is highly potential issue on PSID pin(Q1), a Gate-Source zener for ESD ruggedness, such as FDV301N(Fairchild) is recommended or able to sustain 6KV ESD protection.

+5V\_ALW  
Fsw : 300K  
TDC : 6.52A  
OCP : 10A

+3.3V\_ALW  
Fsw : 375K  
TDC : 3A  
OCP : 4.95A

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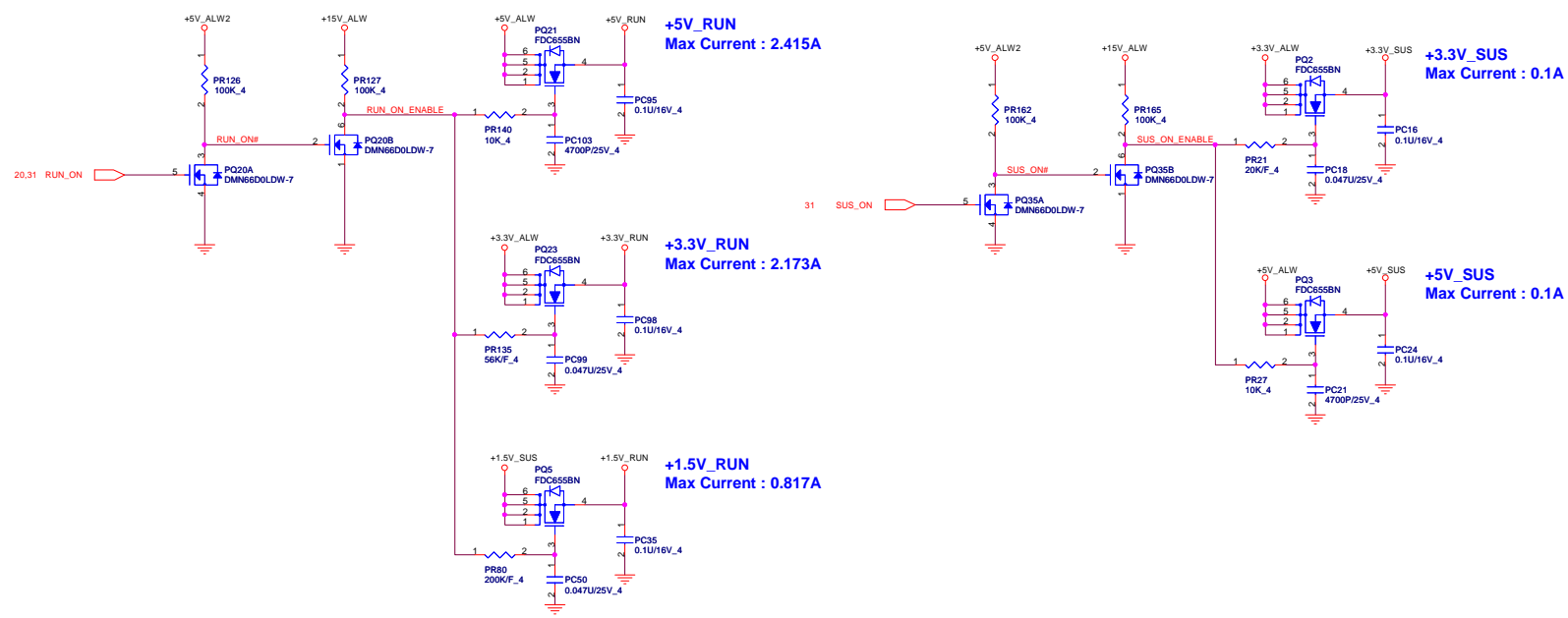
Enable

TPS51125A TONSEL Connection and Switching Frequency				
Ton	REG5	REG3	VREF	GND
Channel1 Fs	365 kHz	300 kHz	245 kHz	200 kHz
Channel2 Fs	460 kHz	375 kHz	305 kHz	250 kHz

P.1. Change PQ30 and PQ31 from FDMC8884 to AON7410, change PR83 to 0ohm  
P.2. Change PQ22 and PQ26 from FDMC8884 to AON7410, change PR151 to 0ohm

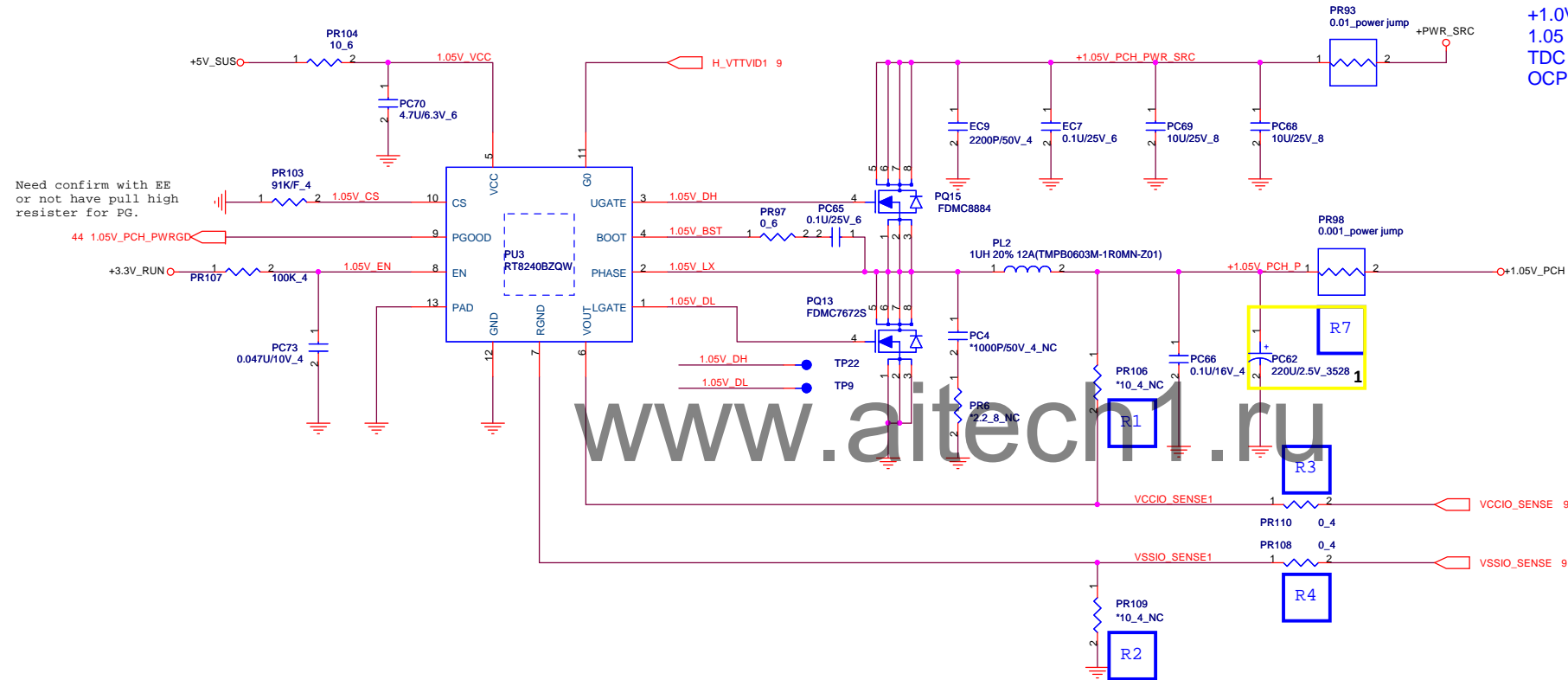






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Need confirm with EE  
or not have pull high  
resistor for PG.

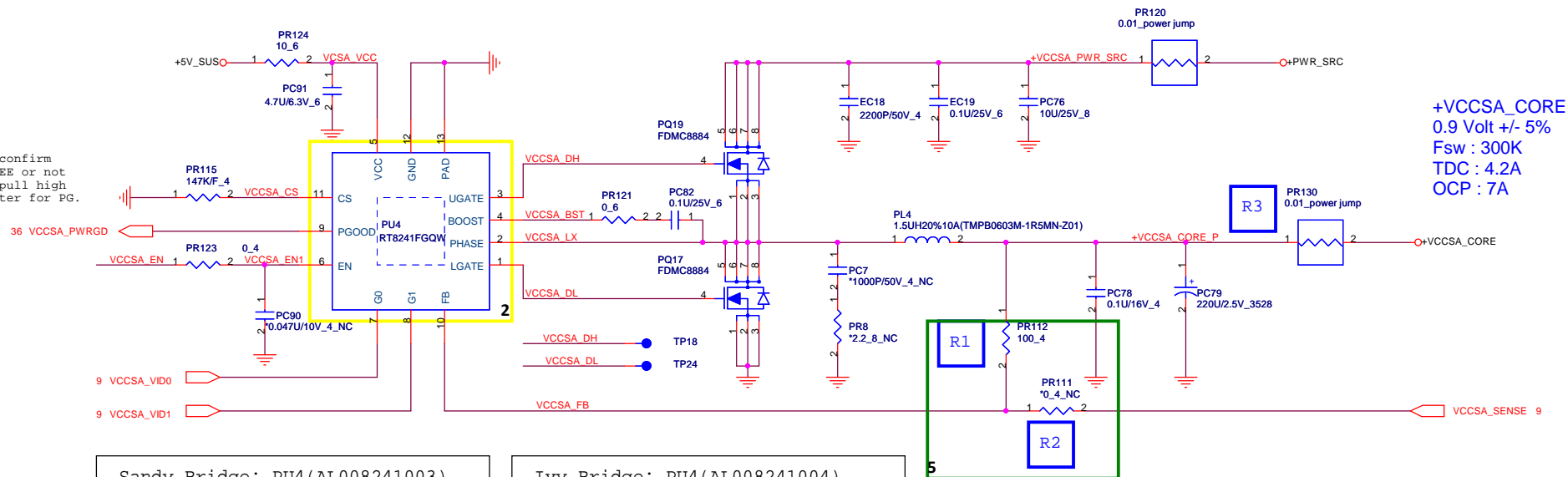


+1.0V\_VCCIO  
1.05 Volt DC +/- 2%  
TDC : 10.669A  
OCP : 16A

For EA test	
R1	10_4
R2	10_4
R3	NC
R4	NC
R5	NC
R6	NC
R7	NC

S\_1. Change PC62 to 220uF/ESR15 for shortage issue

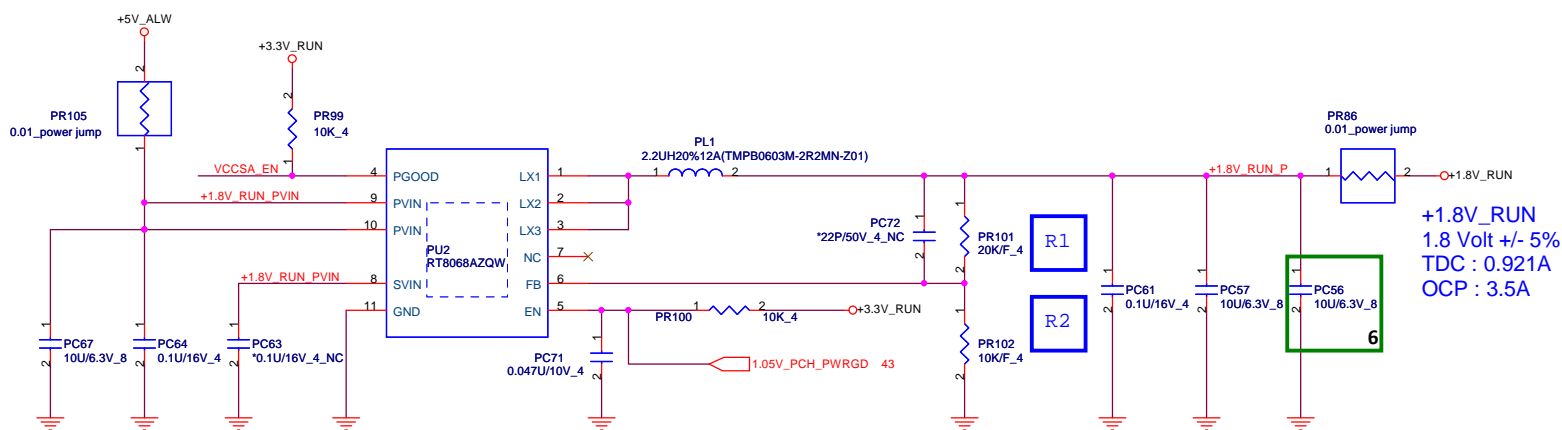
Need confirm  
with EE or not  
have pull high  
resistor for PG.



Sandy Bridge: PU4(AL008241003)		
VCCSA_VID1	VCCSA_VID0	VCCSA_CORE
Low	Low	0.9V
High	Low	0.85V
Low	High	0.725V
High	High	0.675V

Ivy Bridge: PU4(AL008241004)		
VCCSA_VID1	VCCSA_VID0	VCCSA_CORE
Low	Low	0.9V
High	Low	0.85V
Low	High	0.775V
High	High	0.75V

For EA test	
R1	100_4
R2	NC
R3	NC
R4	NC



$$VOUT = 0.6(1+R1/R2)$$

- P\_5. Change to local sense
- P\_6. Pop PC56
- S\_2. Change PU4 P/N for IVB CPU change



Adapter type	65W	90W
ADAPT_TRIP_SET	0	1
SETTING CURRENT	3.7A	5.6A

P\_10. Change PC120 to 10uF.  
S\_1. Add PC137 for input voltage stability.